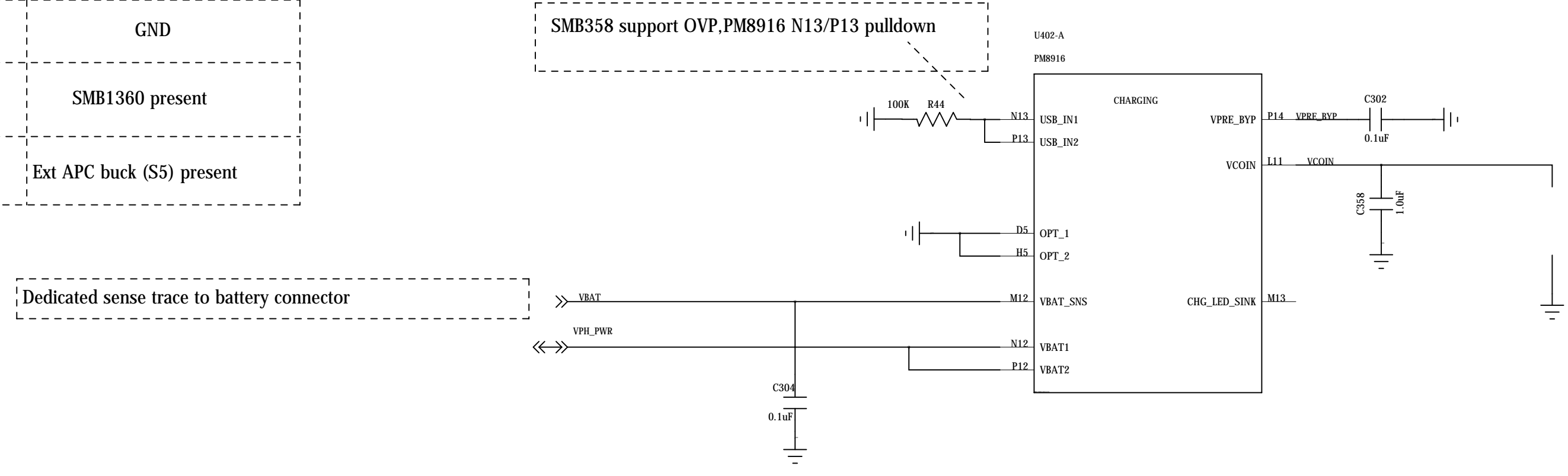
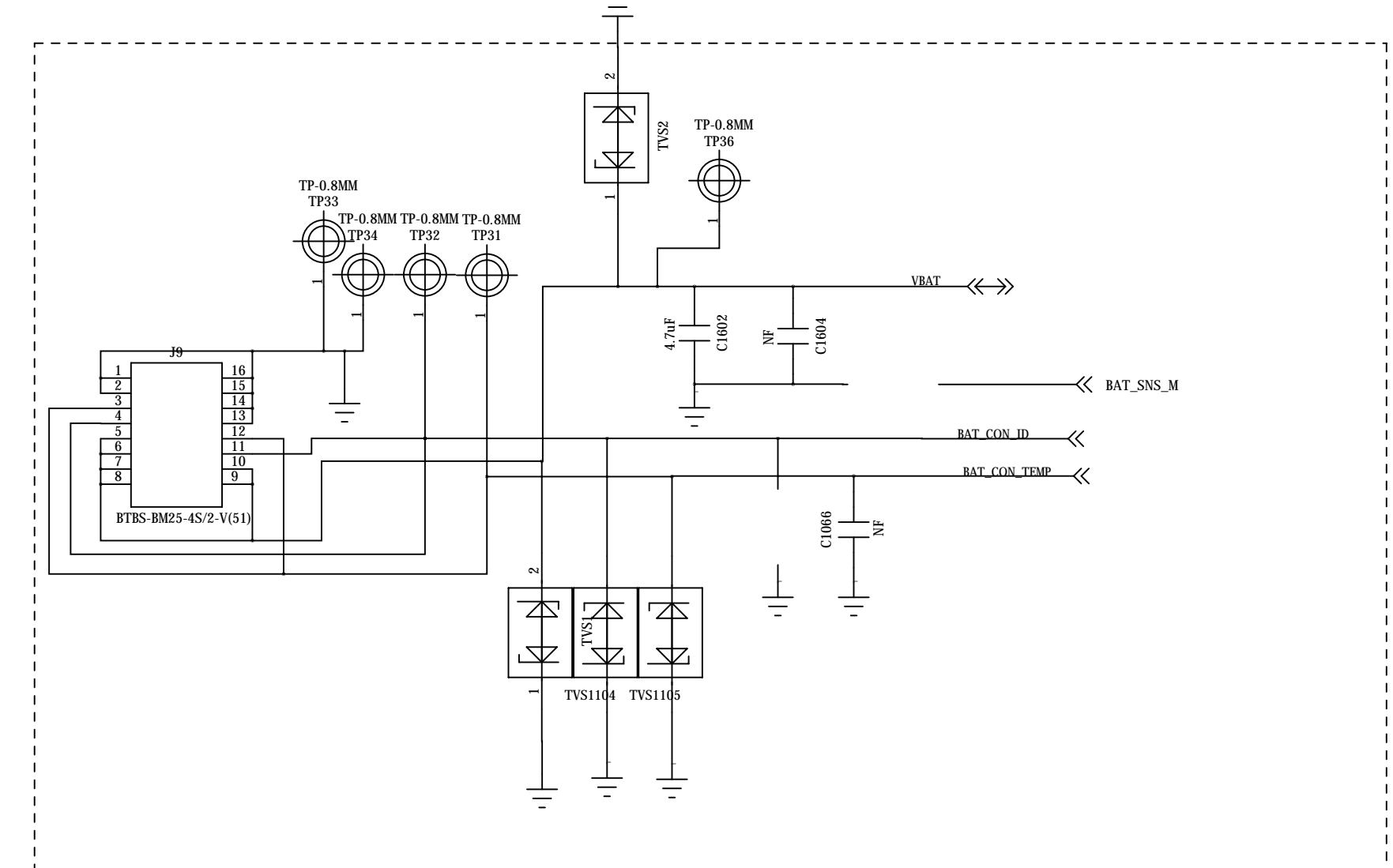
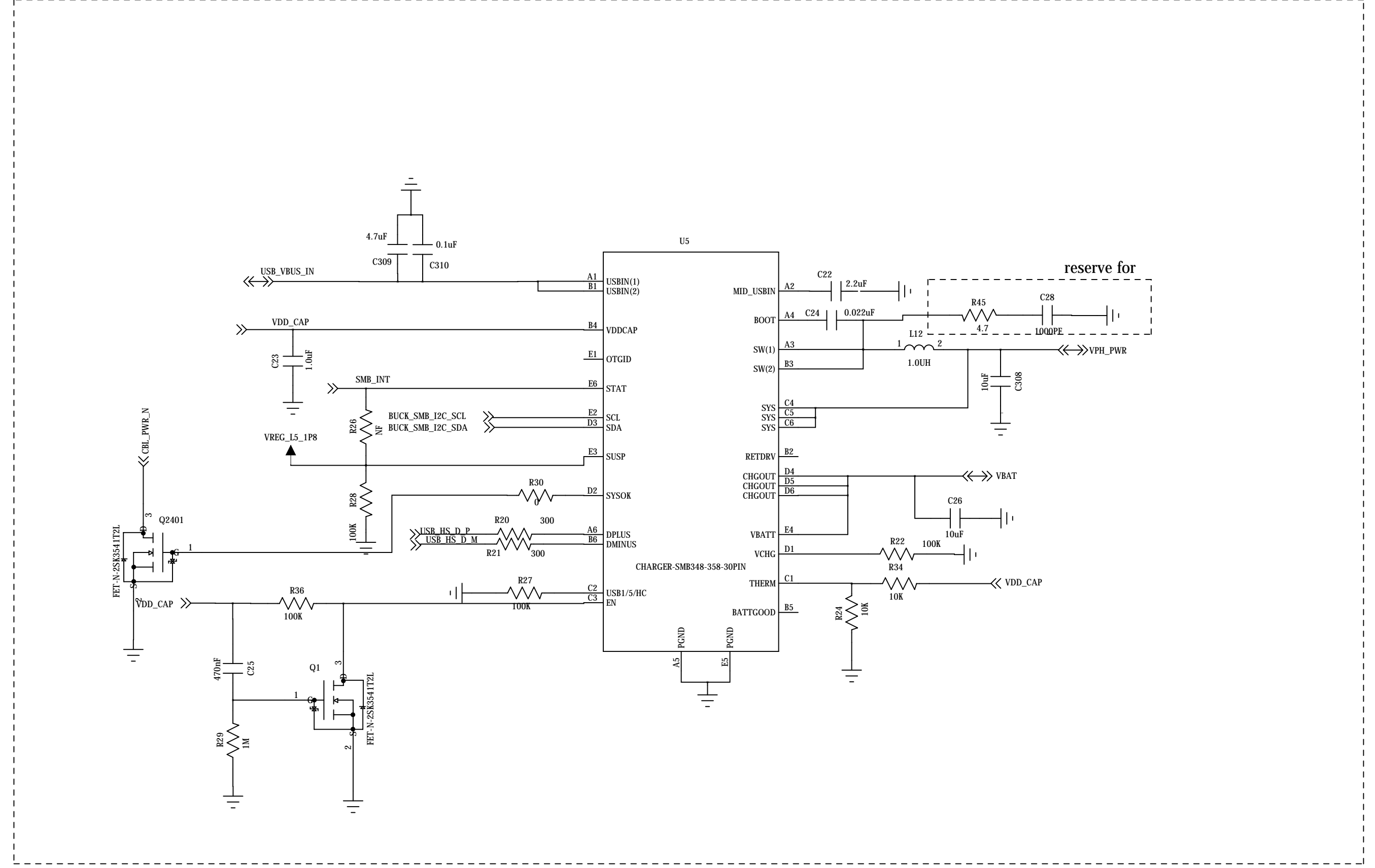
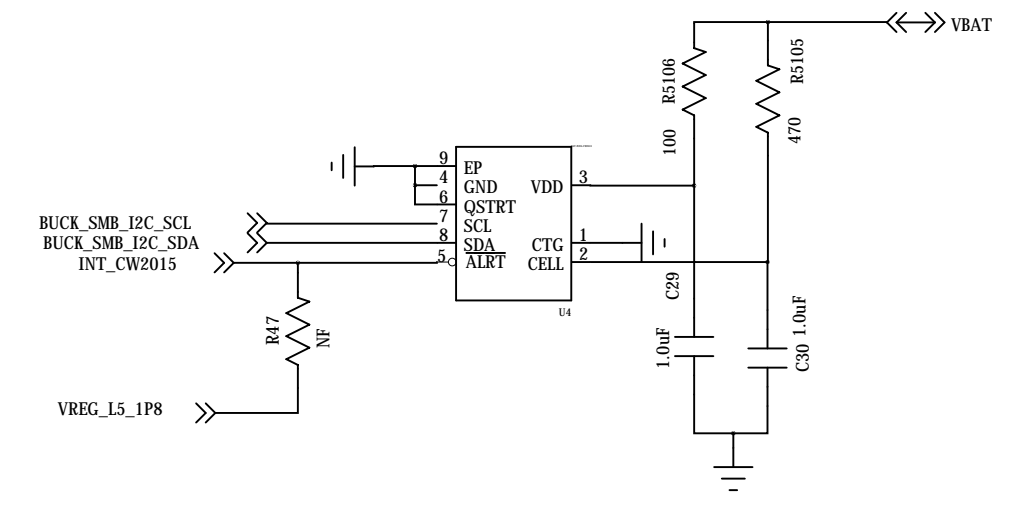


Pins	Hi Z	GND
OPT_1	No SMB1360	SMB1360 present
OPT_2	No Ext APC buck (S5)	Ext APC buck (S5) present



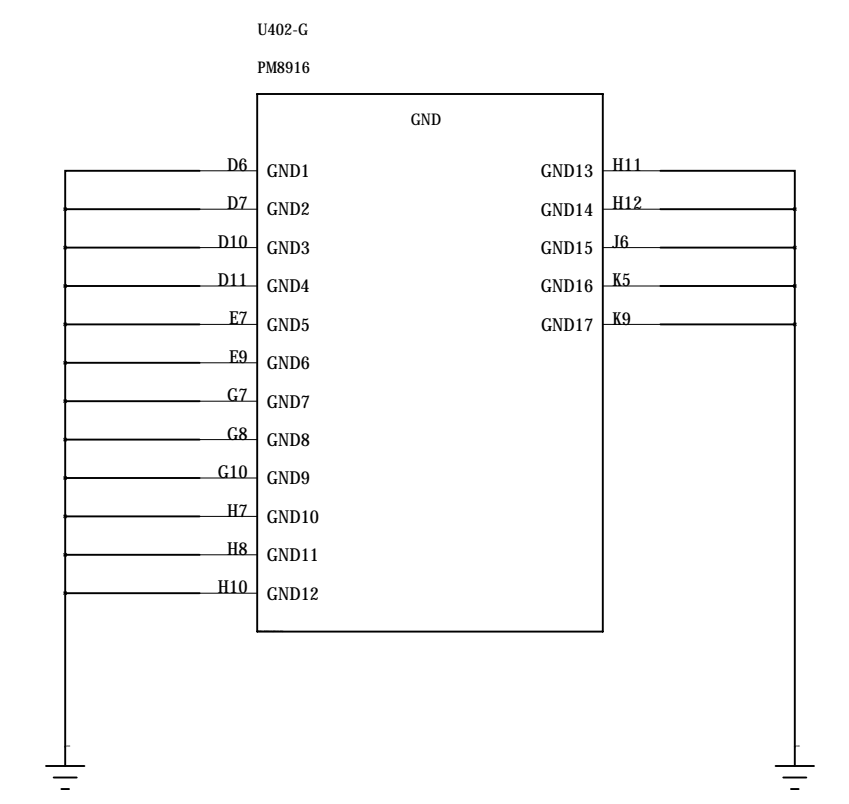
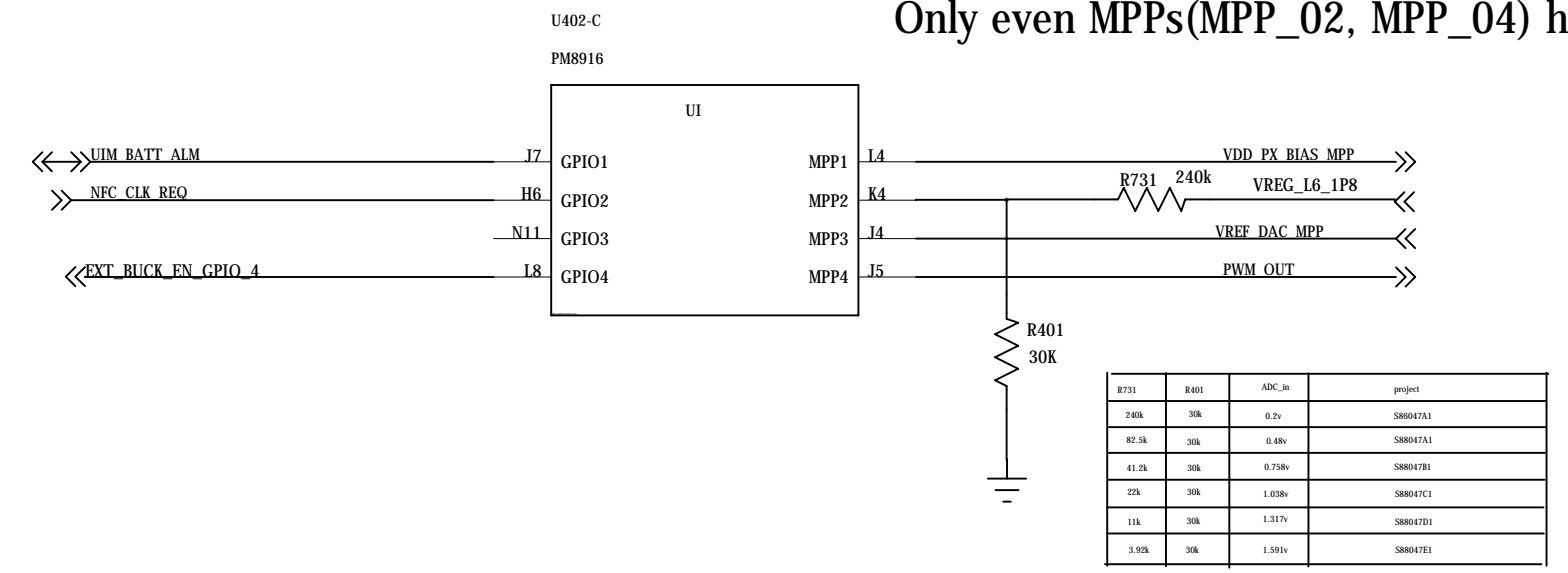
Dedicated sense trace to battery connector

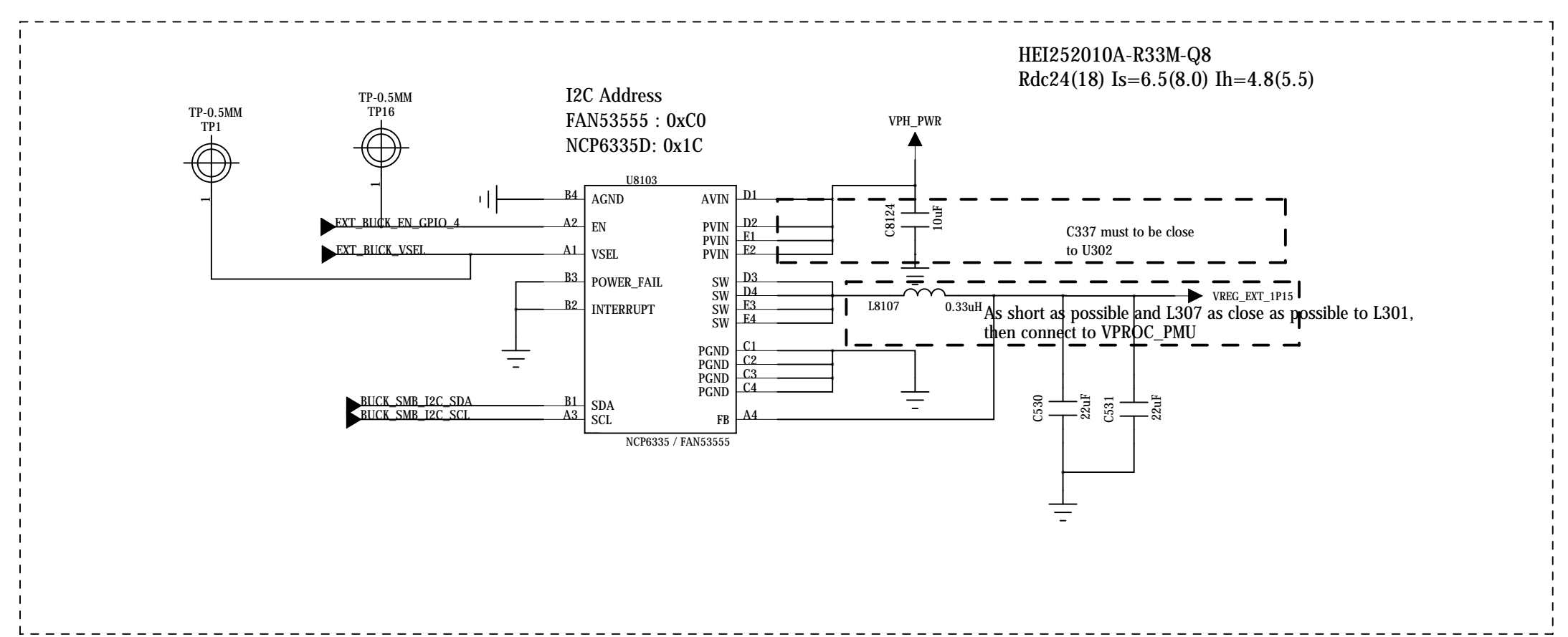
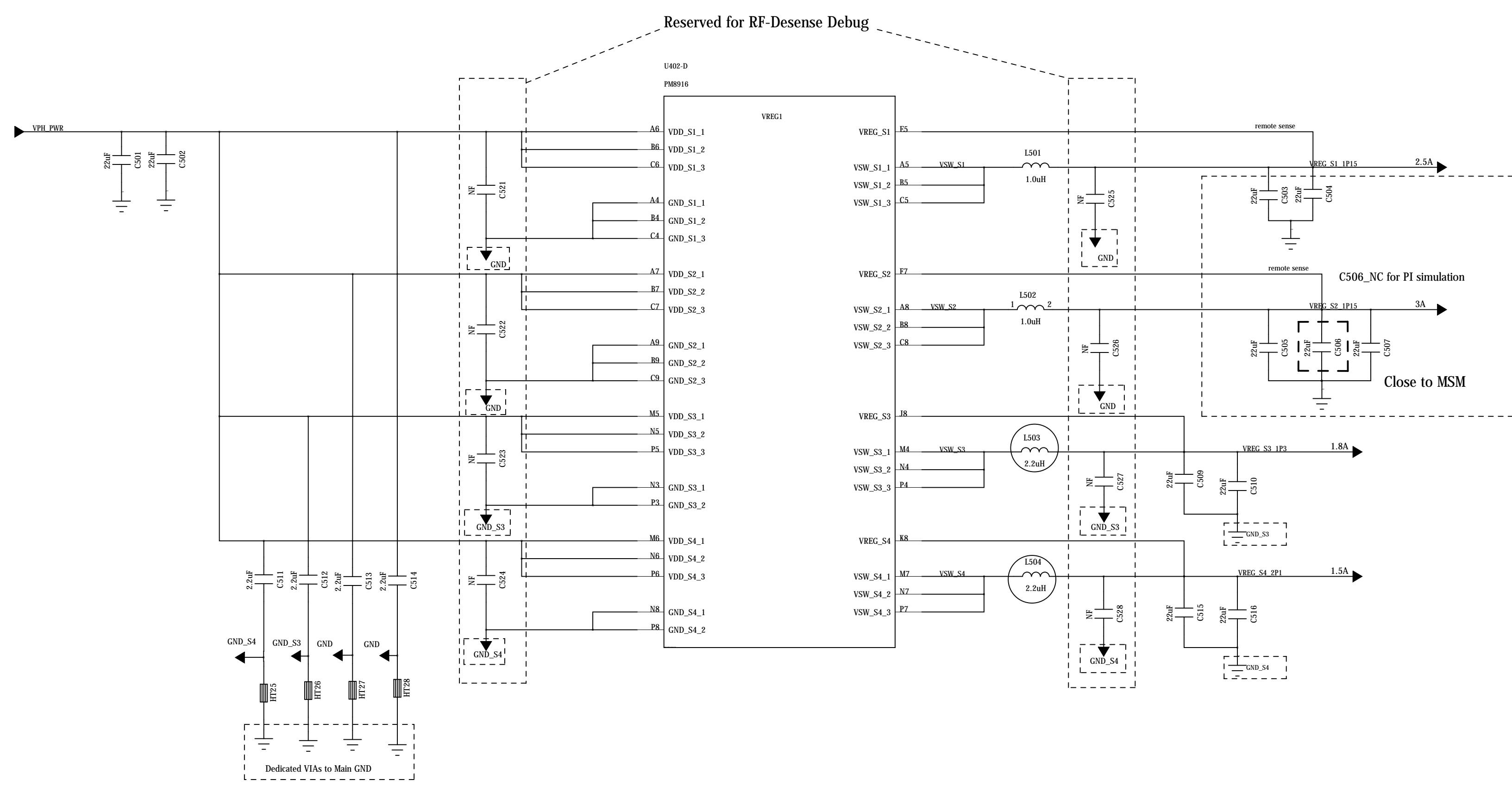
Close to connector if using PMIC's linear charger
 C0301 should assemble 4.7uF/16V capacitor
 R0307 should assemble 0 ohm
 R0302 should NC
 R0312 should be 0ohm
 BAT THERM switch to PM8916

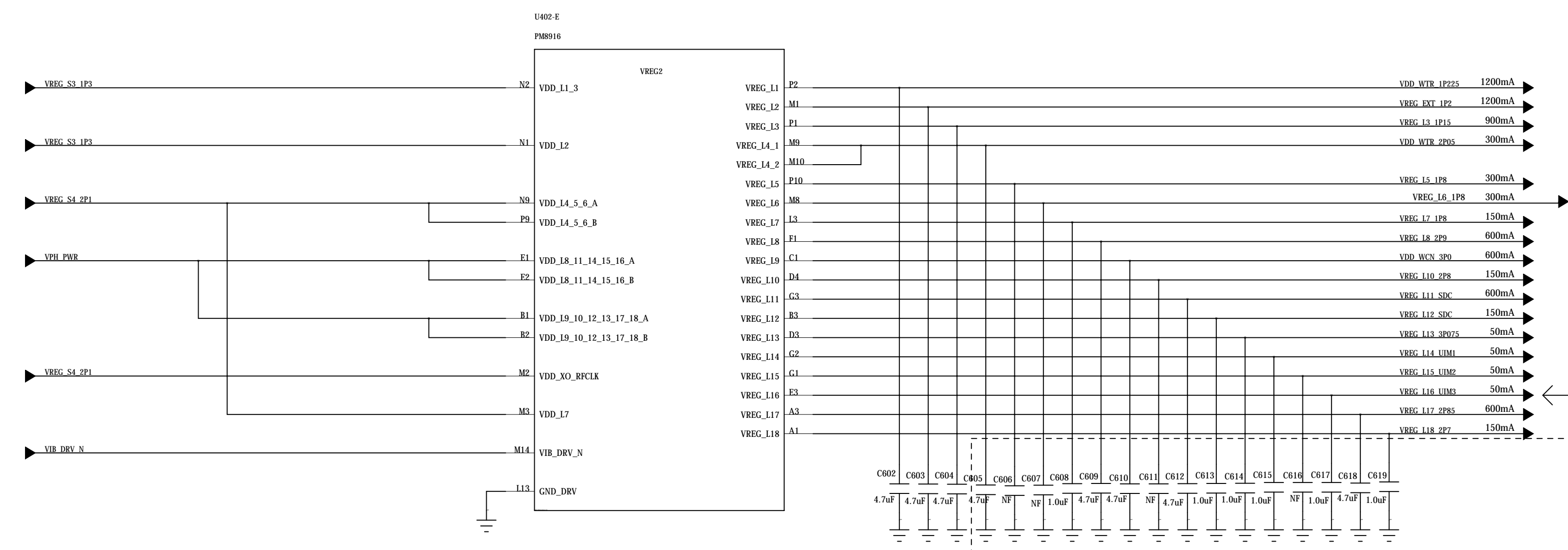


BATTERY CONNECTOR

Only odd MPPs (MPP_01, MPP_03) can be configured as analog outputs.
 Only even MPPs (MPP_02, MPP_04) have current sink capability.







Software Caution:
L16 Need to Config to 1.8V and turn on later than L17

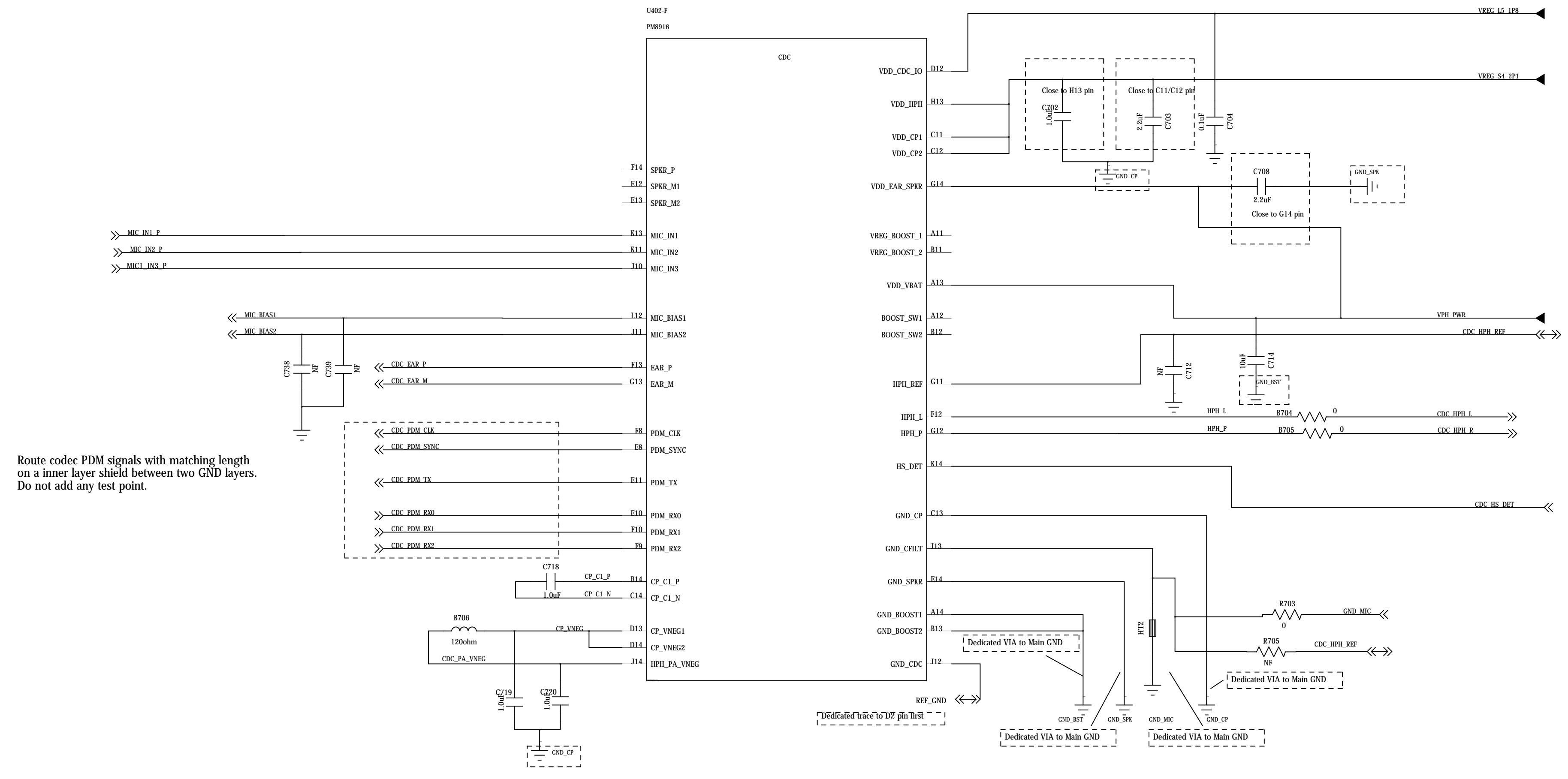
PSEUDO CAPLESS LDOs
L4, L5, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18

Local output capacitor can NC/Remove depends on remote load capacitors and PCB layout
LDOs L8, L9, L11, L17 each shall have total effective output capacitance of 4.7uF.
Please refer to PM8916 training slides(80-NK808-21) for limits on LDO output trace resistance and inductance
Rest of the LDOs shall each have total effective output capacitance of 1.0uF.

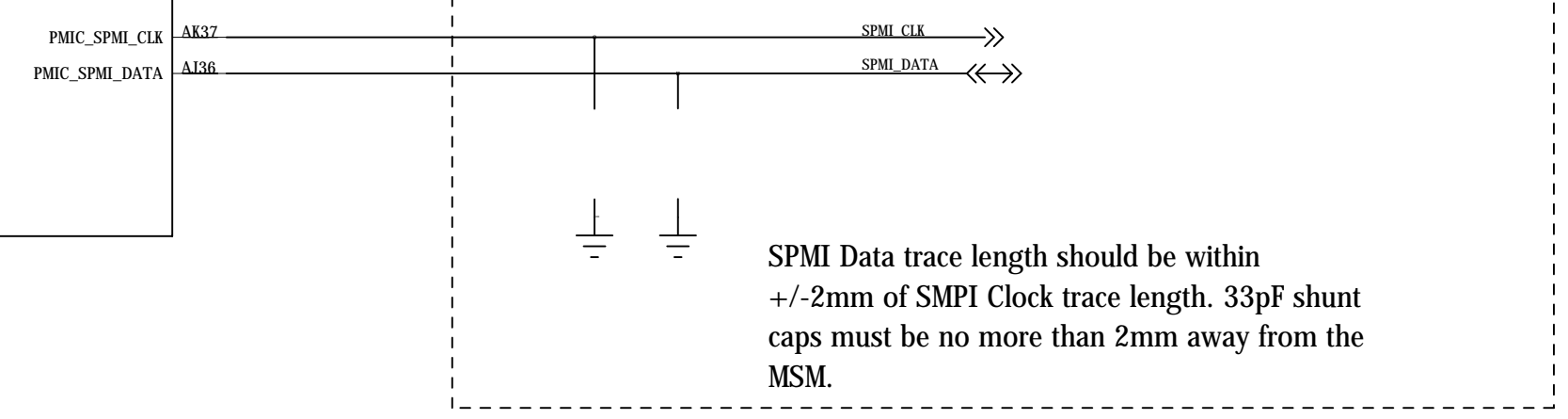
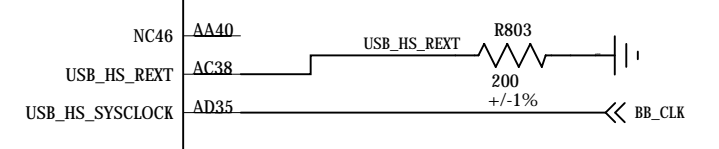
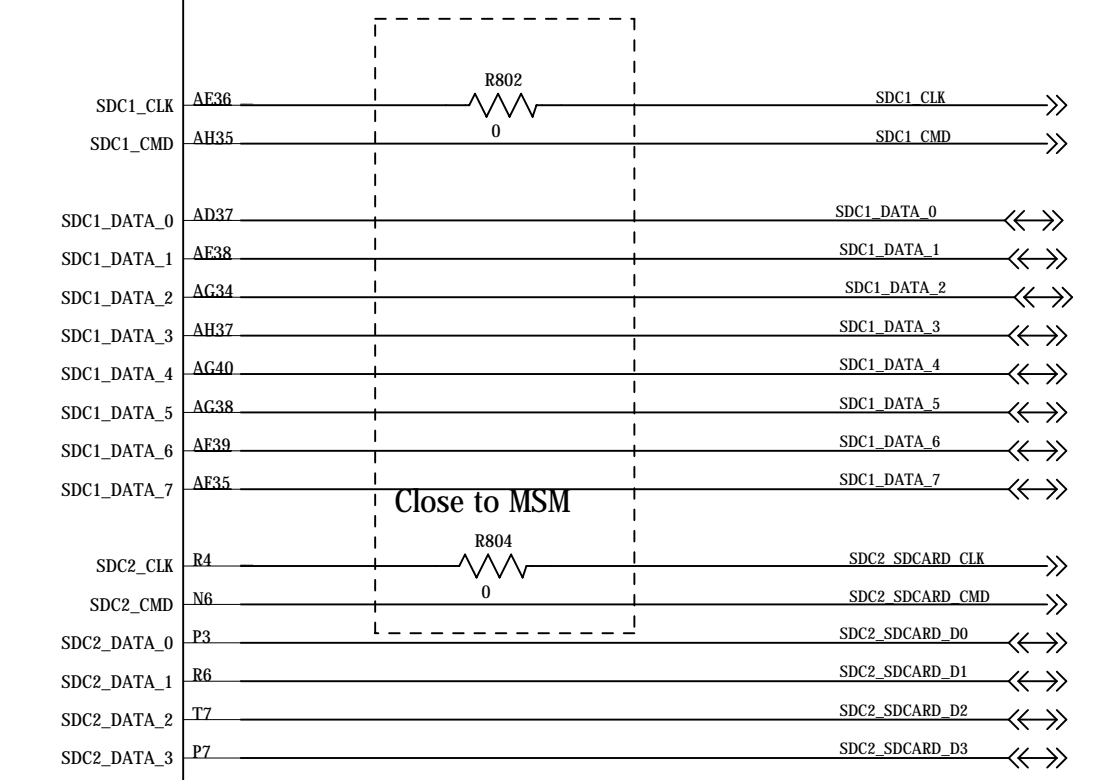
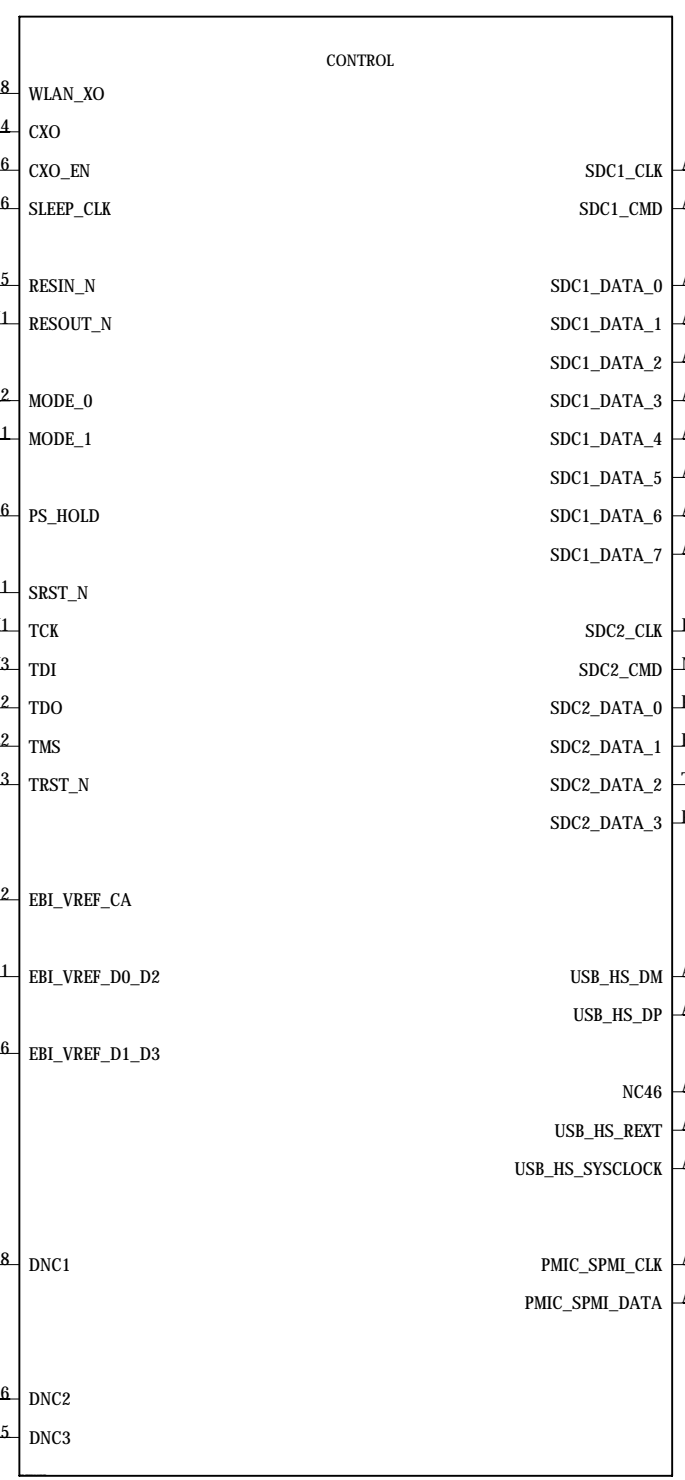
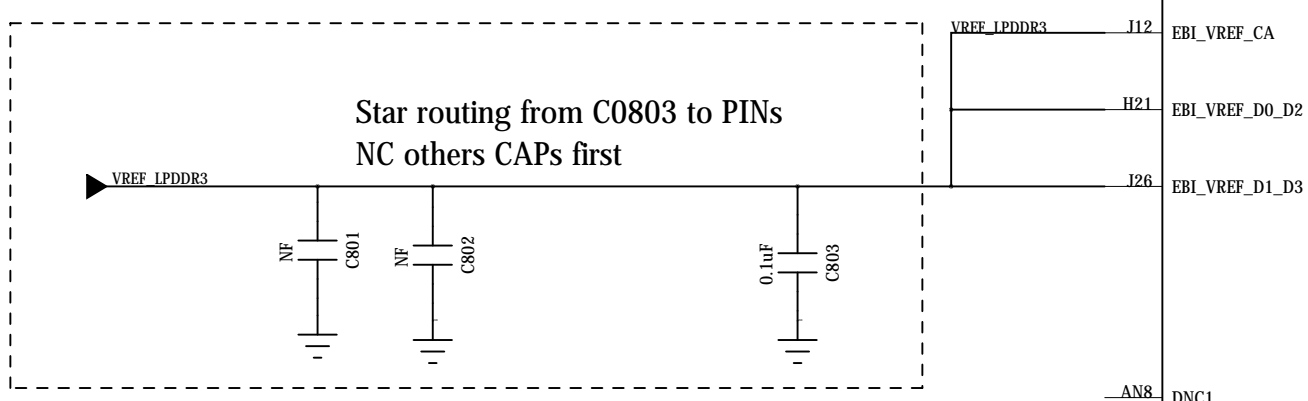
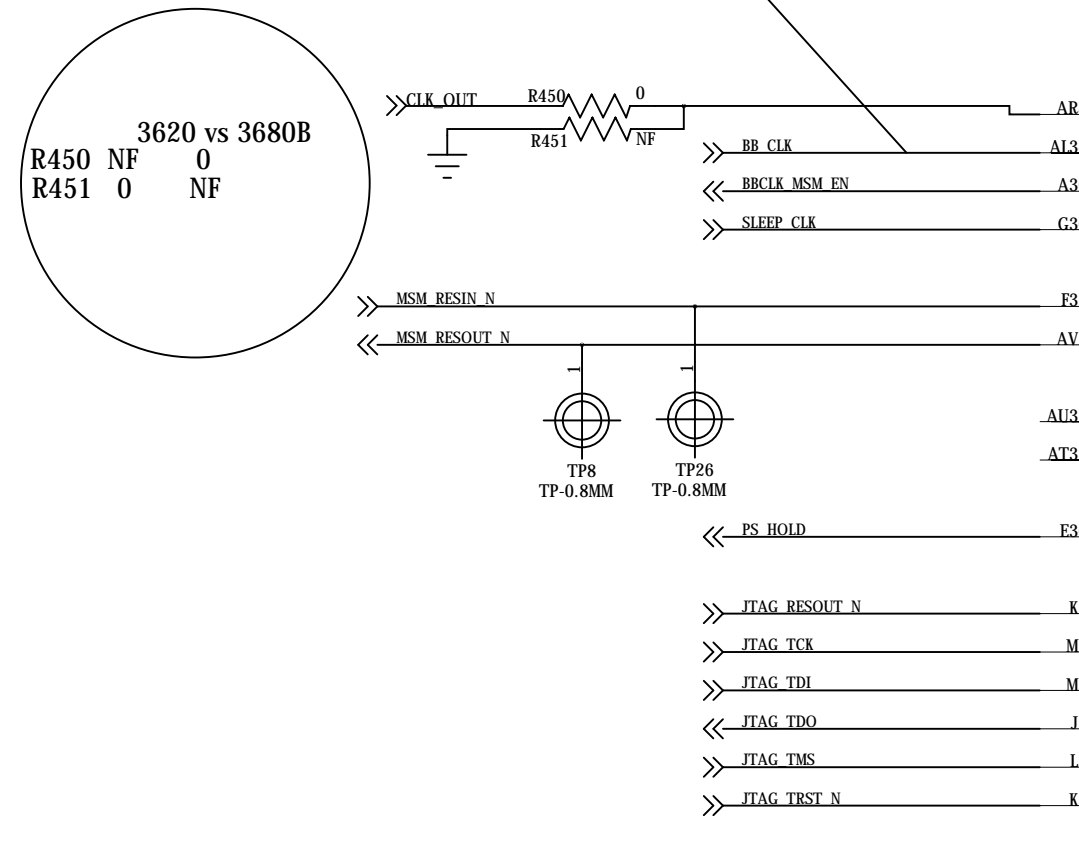
The Pseudo capless LDOs must comply to following tolerable routing requirement:
P50: R<400mOhms, L<45nH
P150: R<200mOhms, L<20nH
P300: R<150mOhms, L<18nH
P600: R<150mOhms, L<18nH

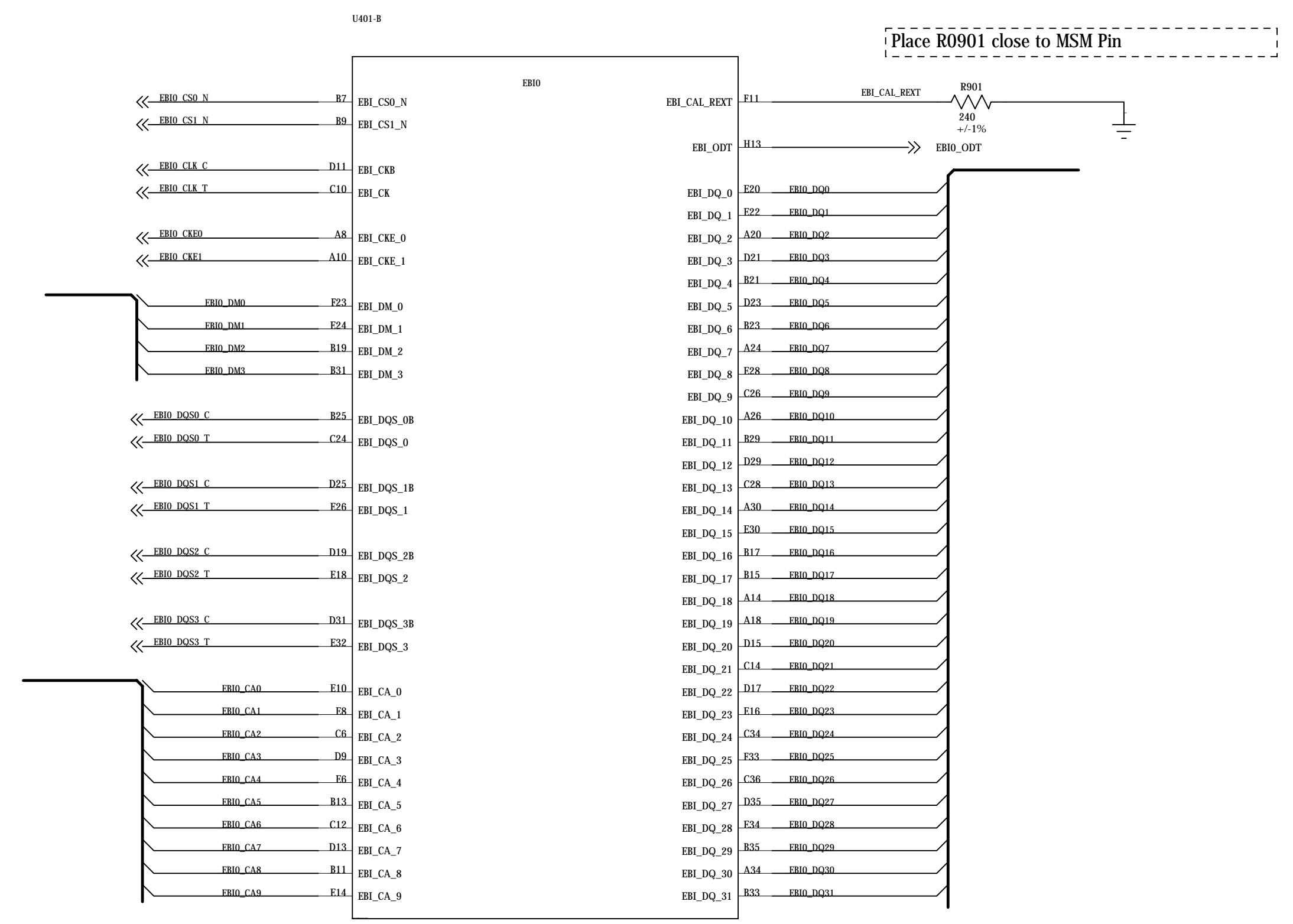
Please ensure when you DNI the output capacitor of Pseudo capless LDOs
the effective total capacitance at load side shall match above requirement

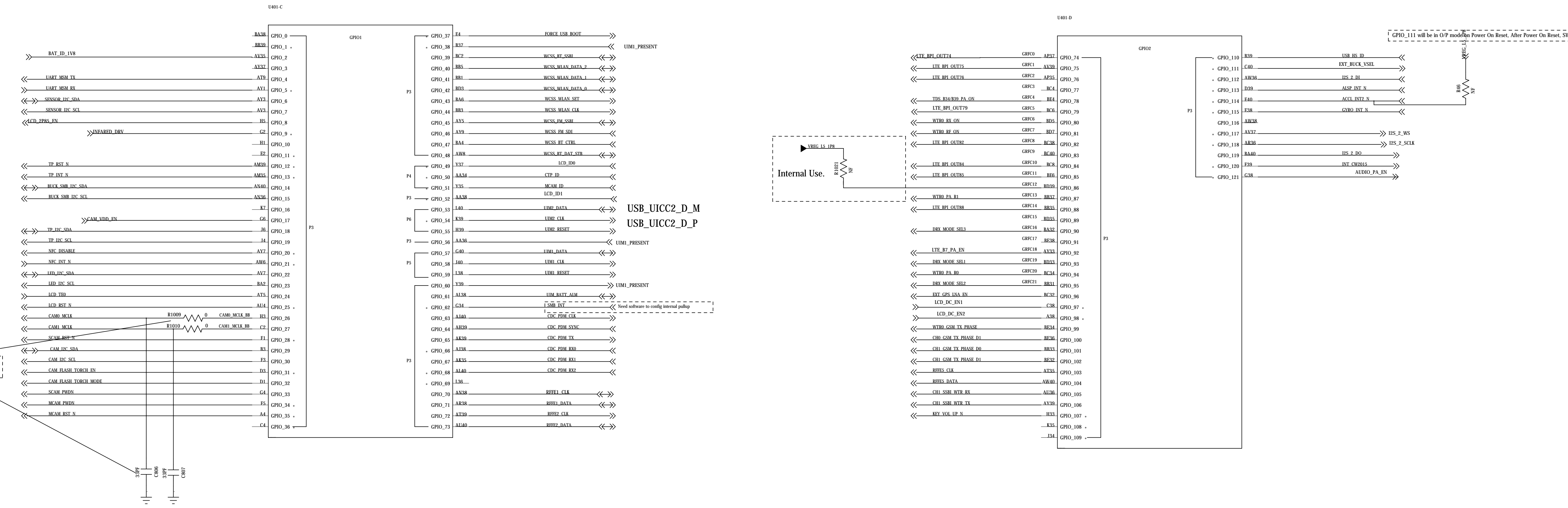
NC first



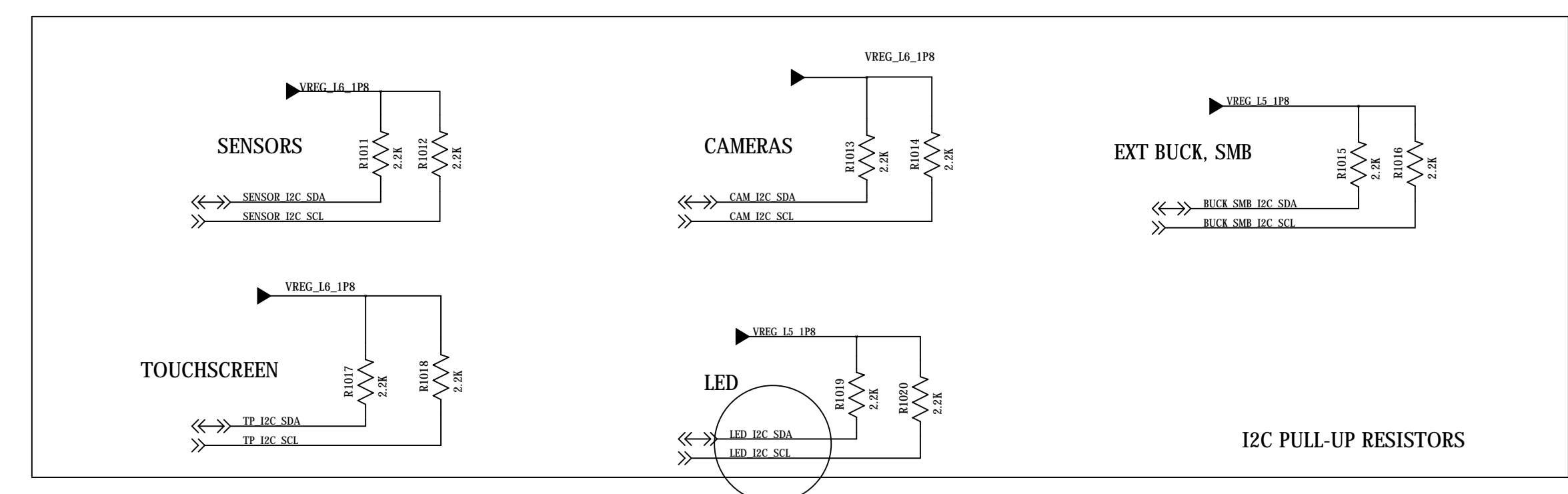
For BBCLK1,AD35 will be the first load and AL34 will be the final load
Should be a daisy chain route

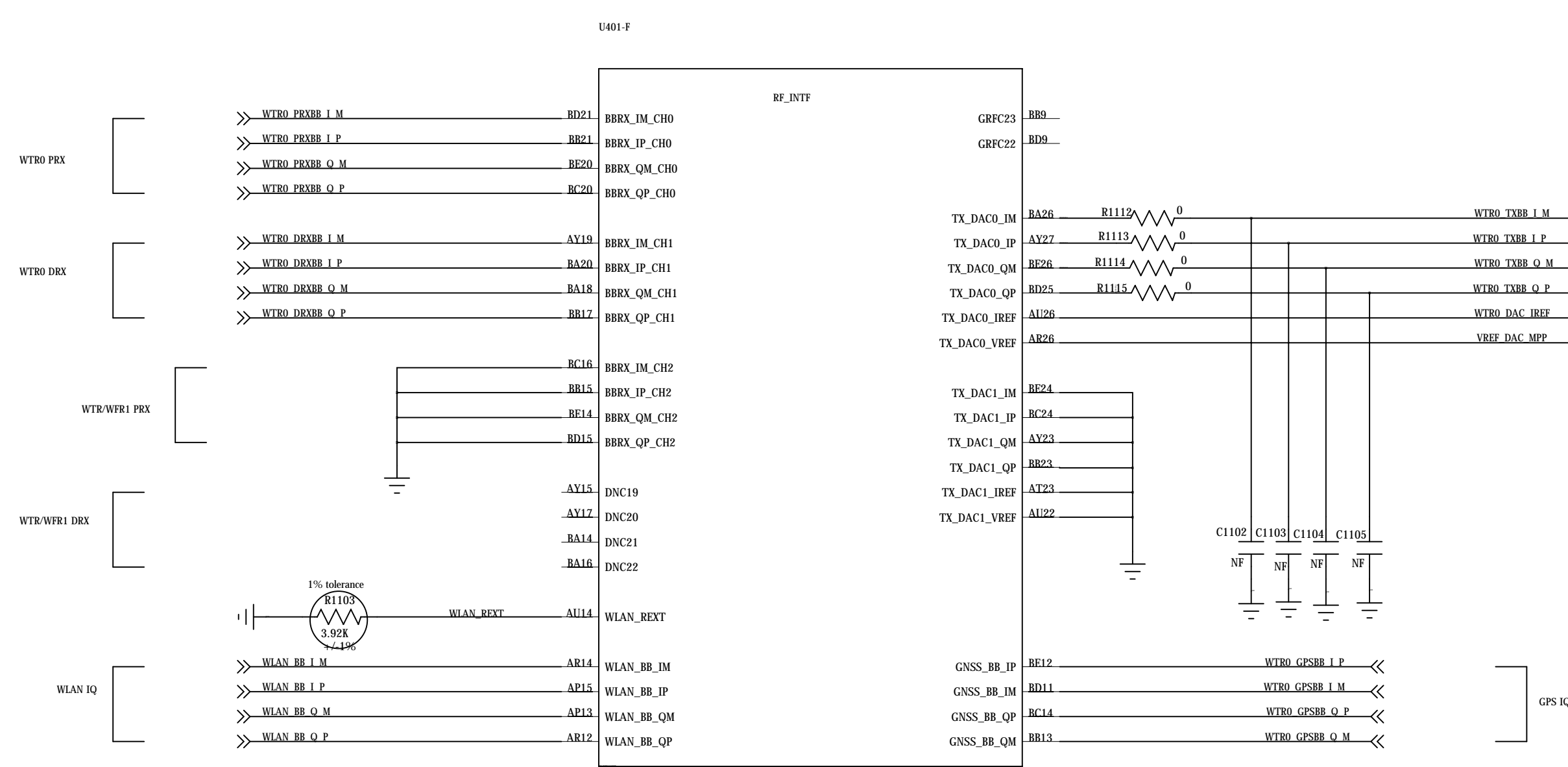
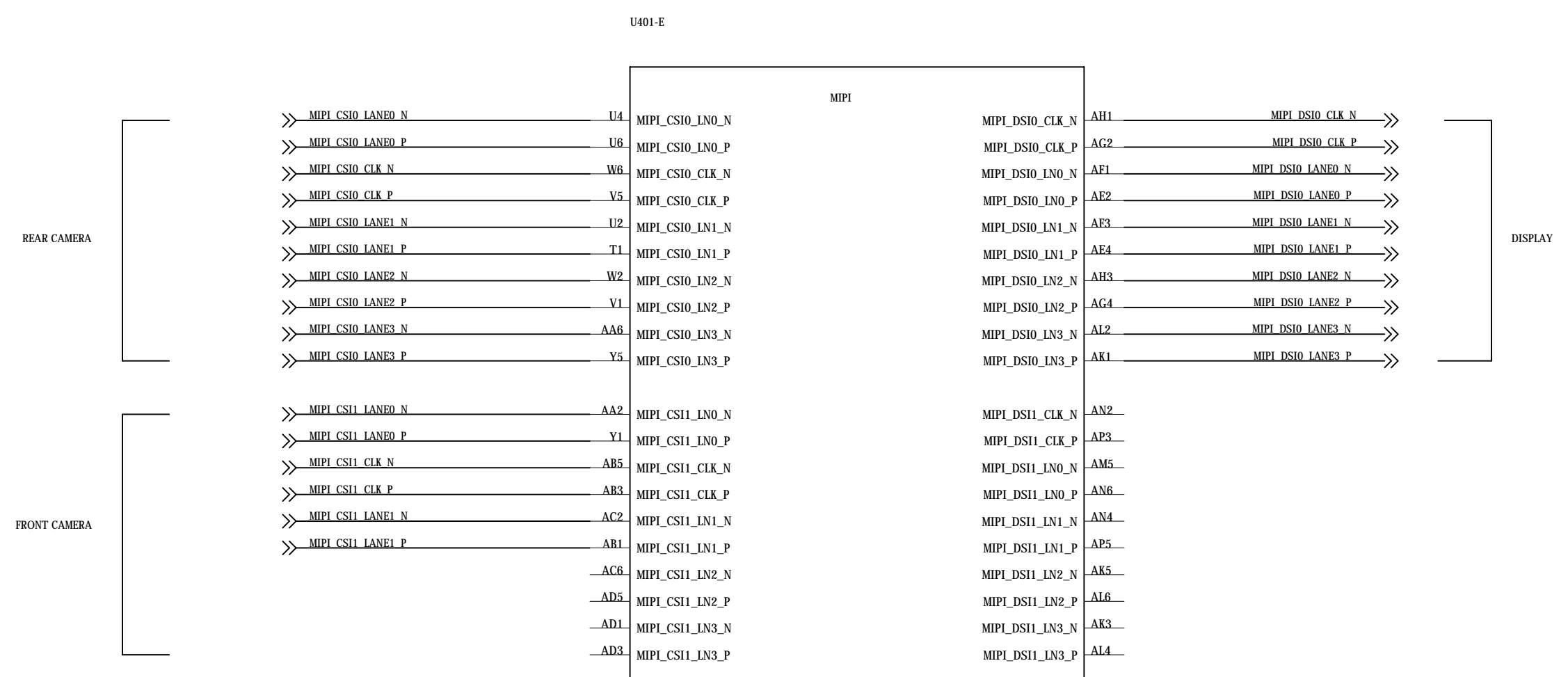






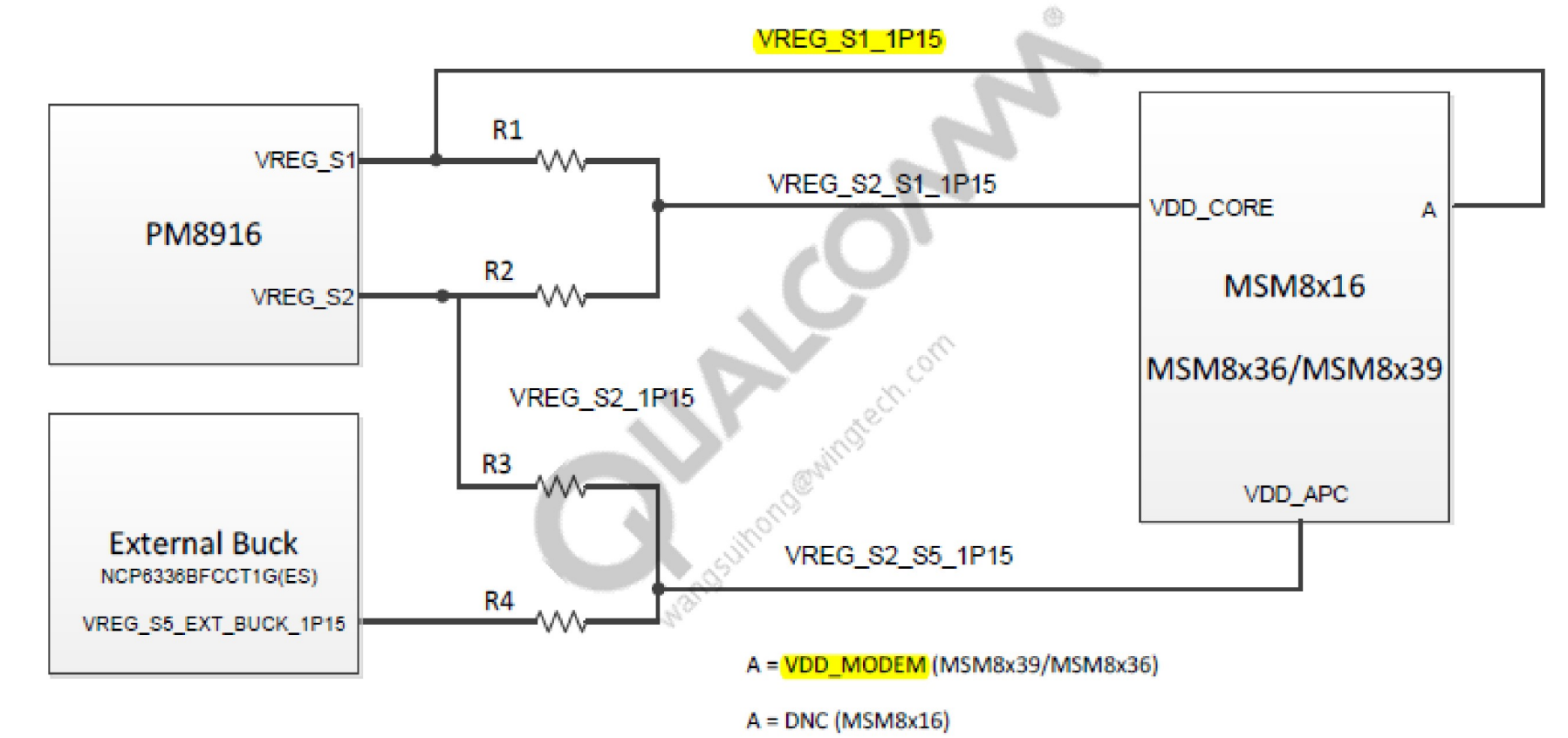
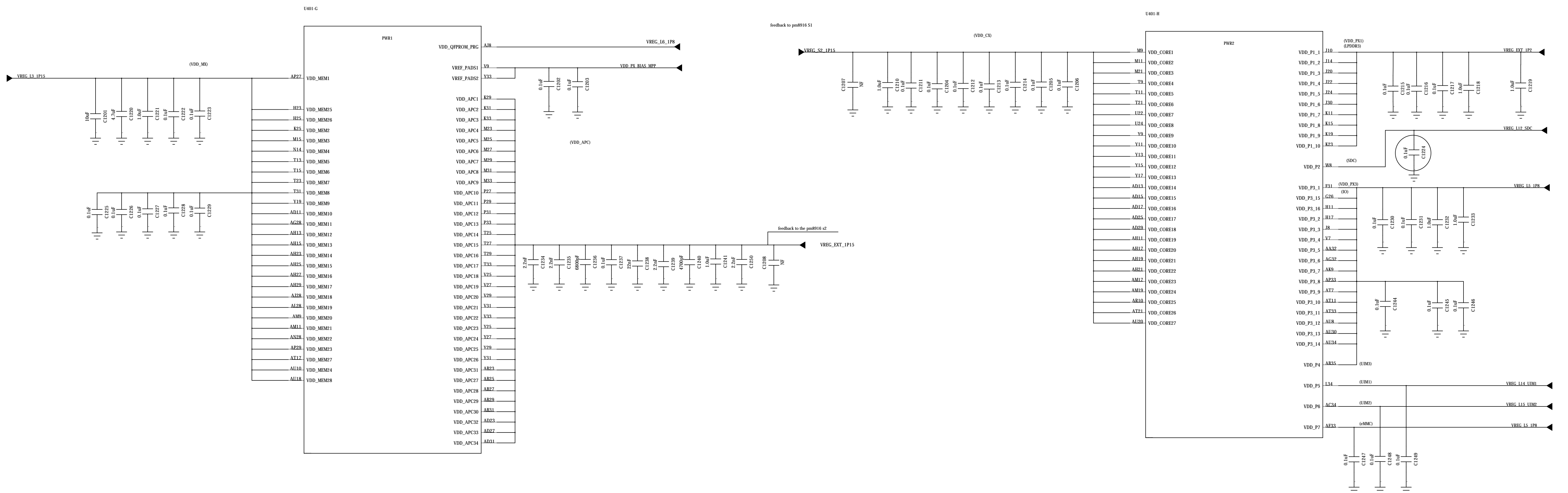
For RF De-sense Debug





	SVLTE, DSDA	OTHERS
R1102	0OHM	NC
R1120	NC	0OHM

These NC resistor is for SVLTE or DSDA. Change them to 0ohm on other modes.



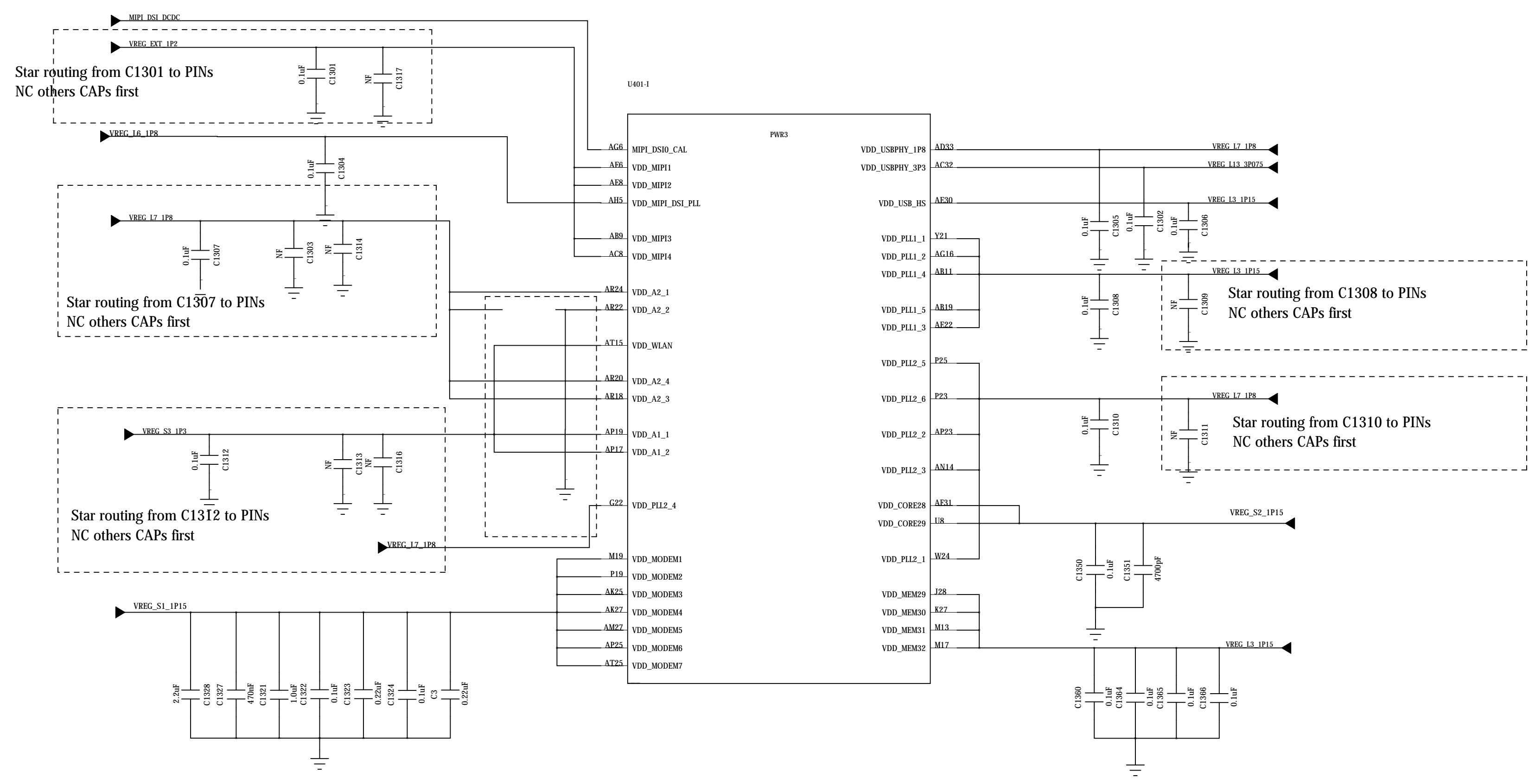
SoC	Jumper on	Jumper off
MSM8x16	R1, R3	R2, R4
MSM8x36/MSM8x39	R2, R4	R1, R3

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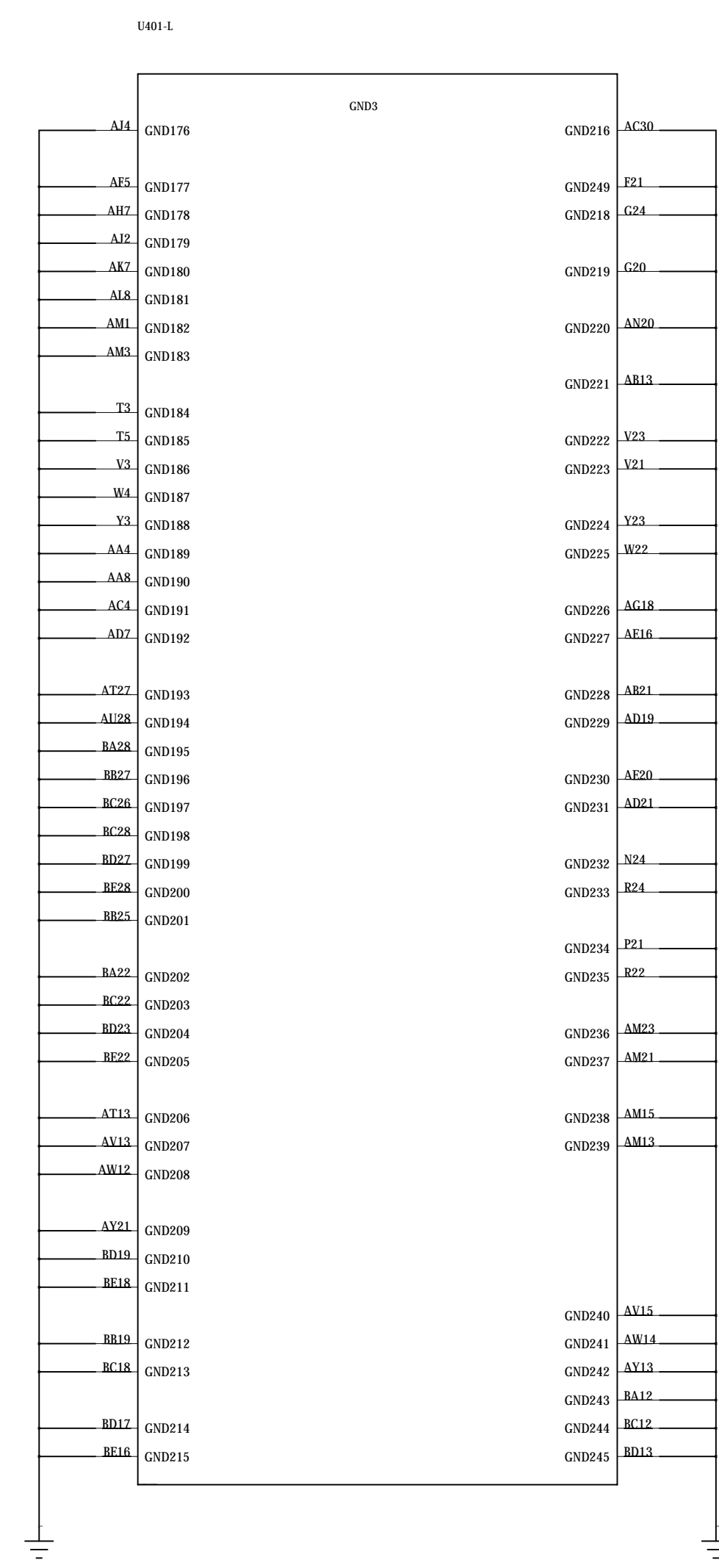
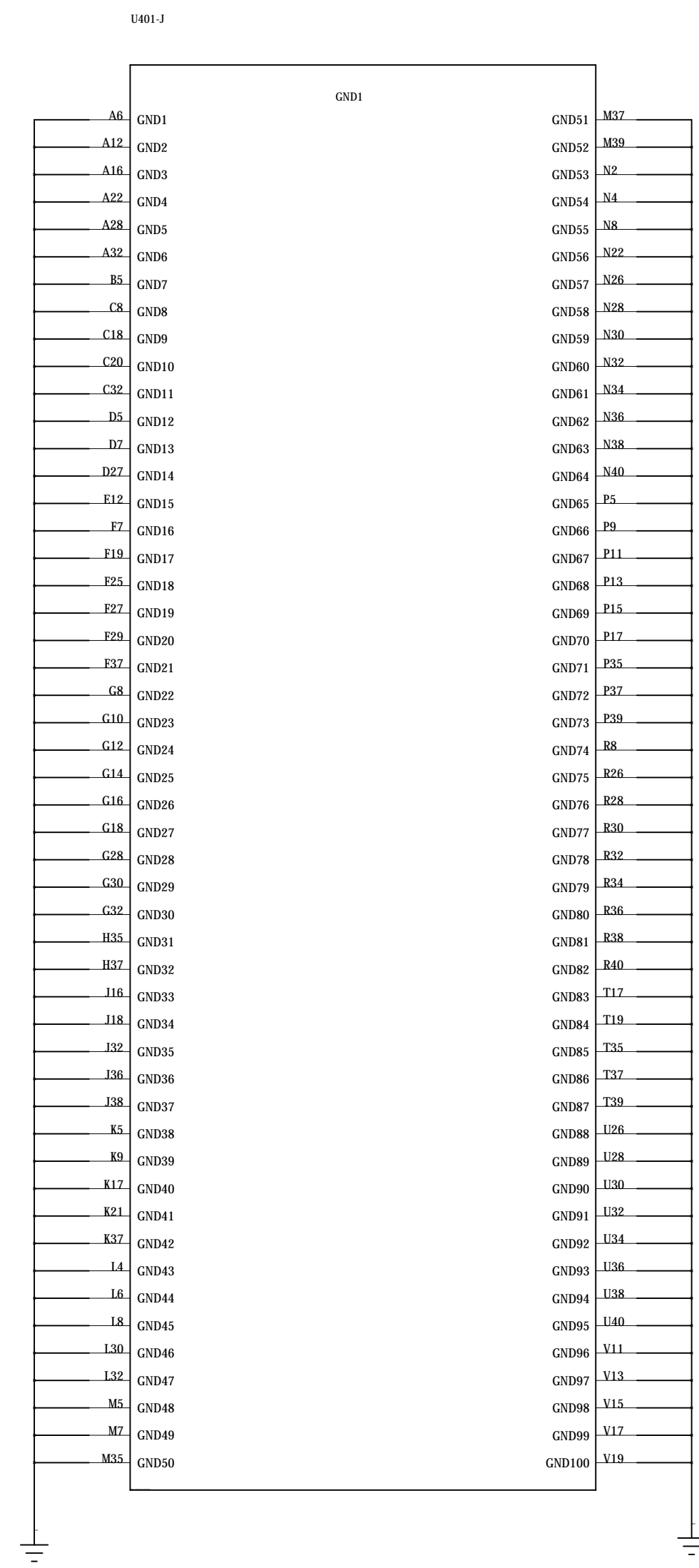
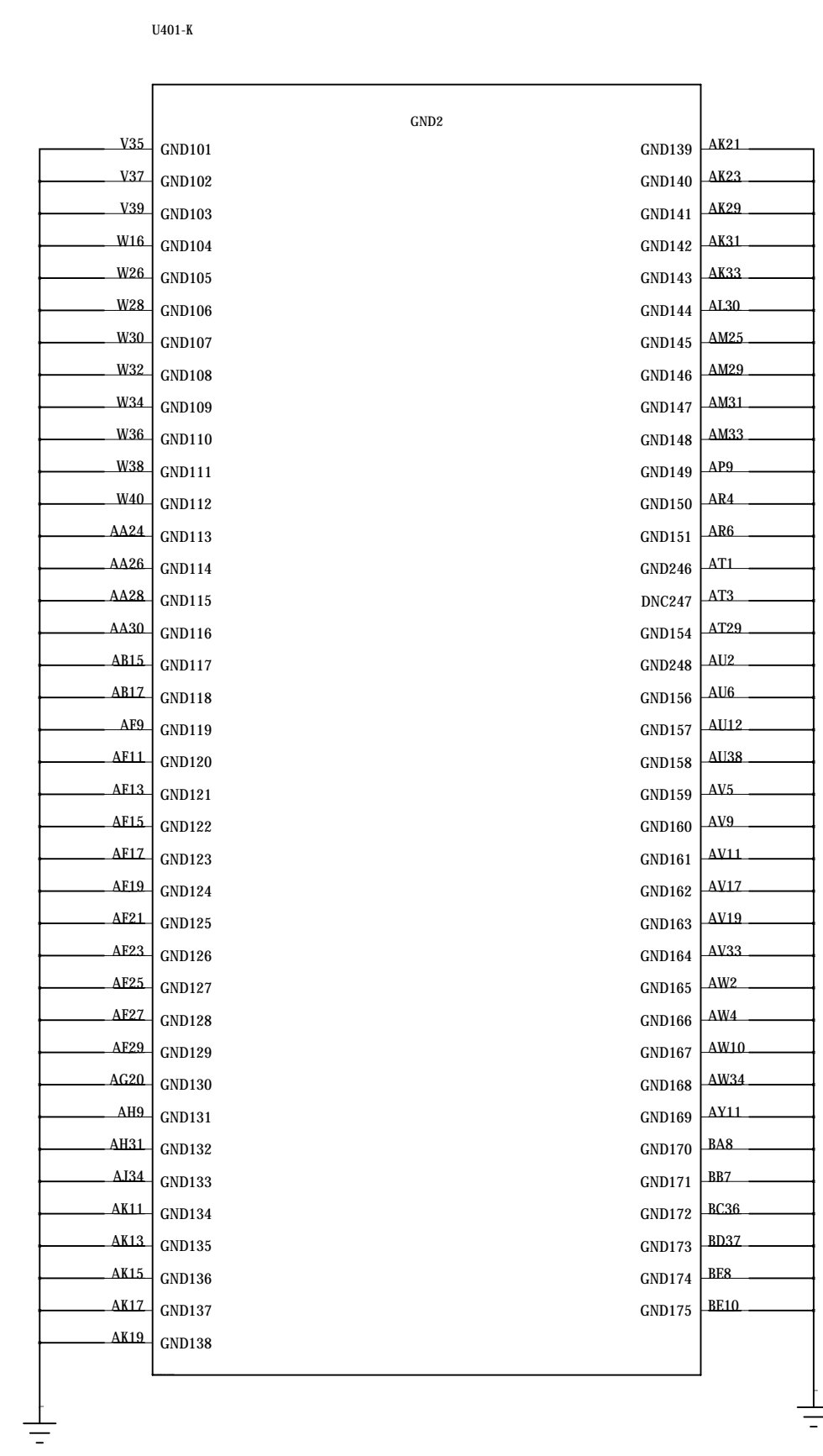
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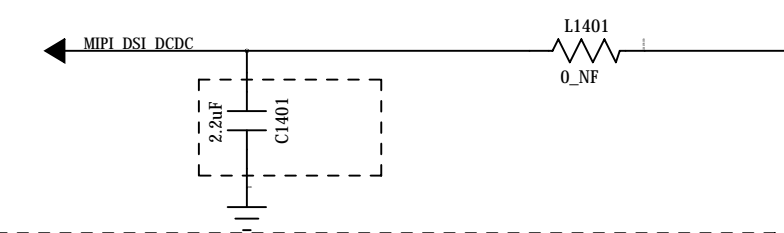
Size: _____ Sheet: _____ Rev: _____



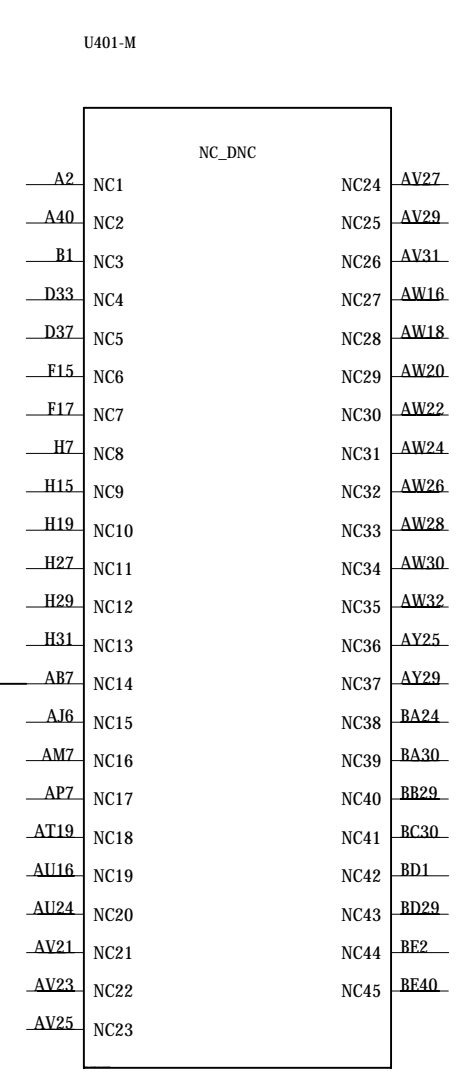
	SVLTD.DSDA	OTHERS
R1301	0OHM	NC
R1302	NC	0OHM



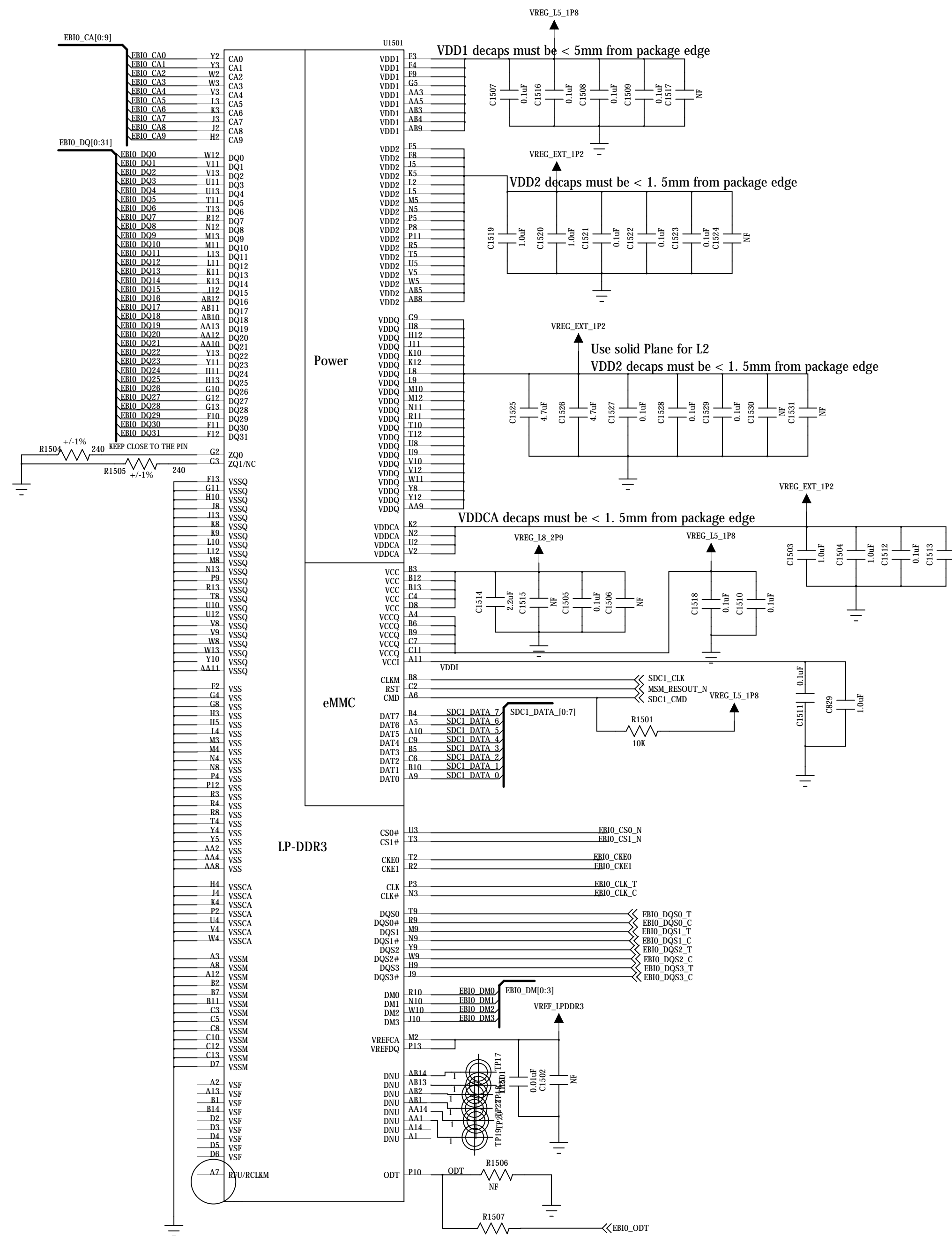
MIPI_DSI_LDO is configured to be LDO mode defaultly, if using DC/DC mode, L1401 need to be replaced with 2.2uH inductor



CAD NOTE: Loop to be shorted with MSM AB7 pin



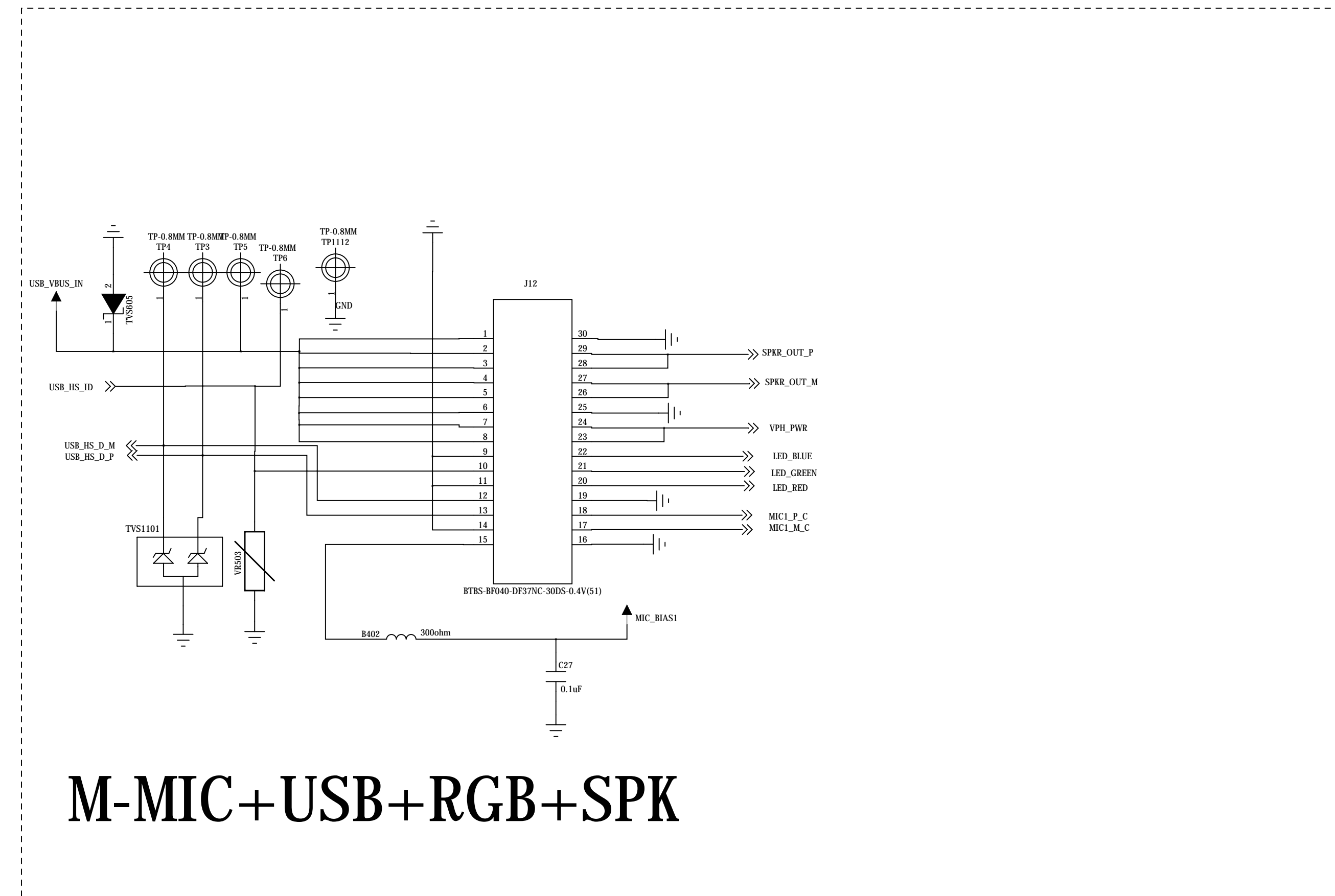
	MICRO/HYNIX	SAMSUNG
U1501.G3	ZQ1	NC
U1501.A7	RFU	RCLK



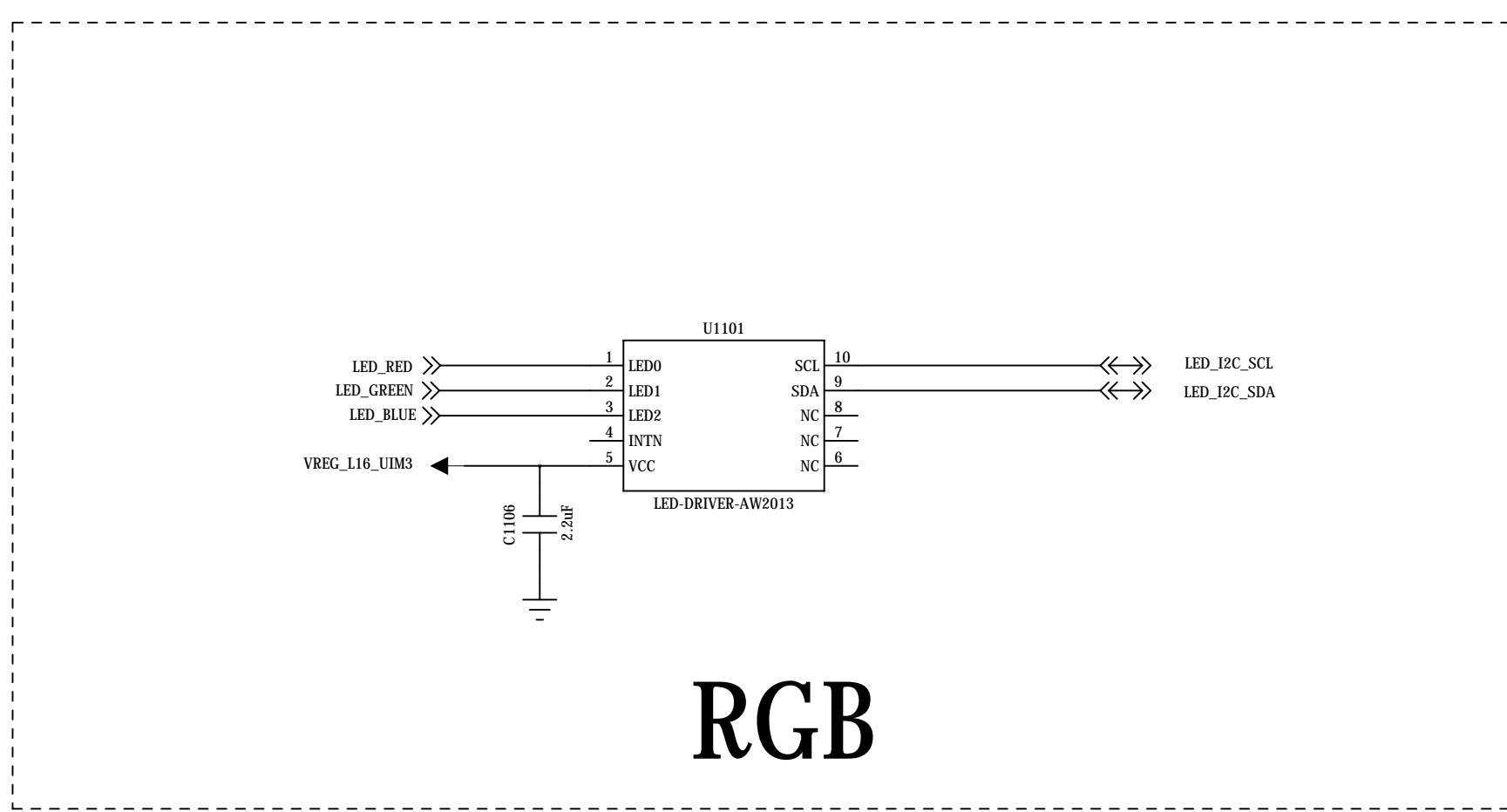
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Size	Rev
Sheet	of



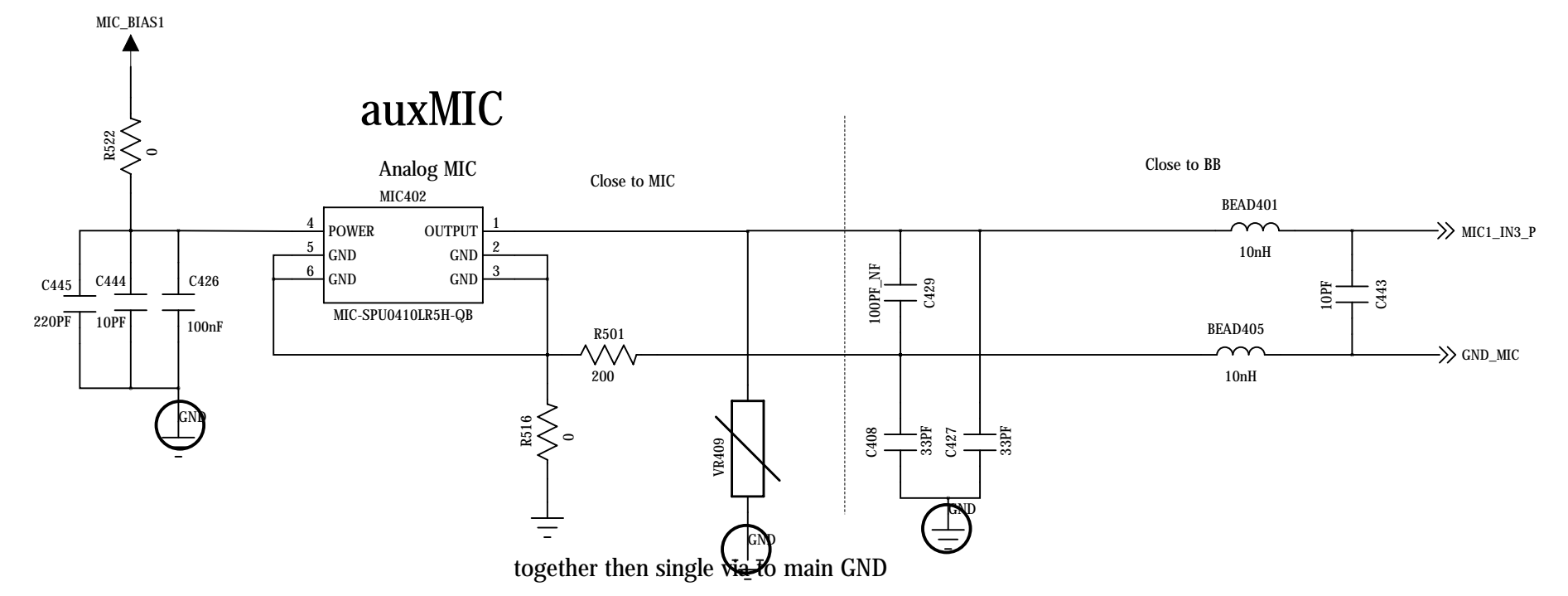
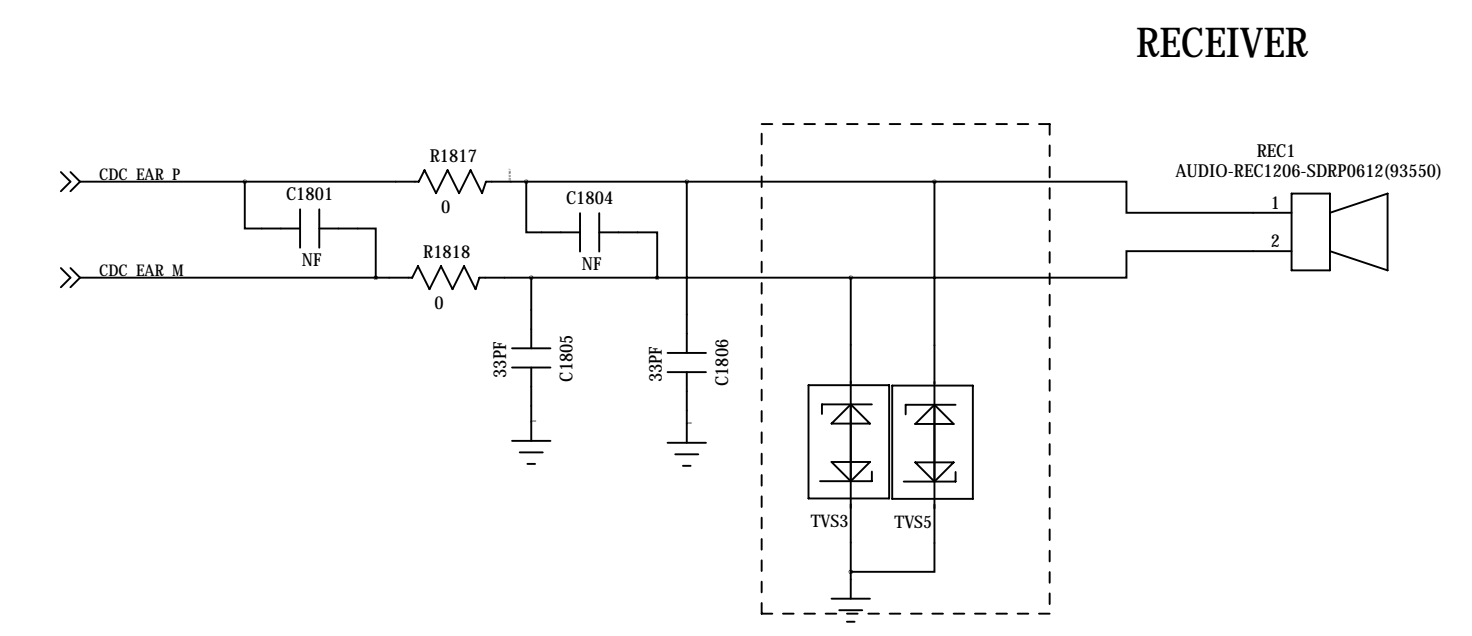
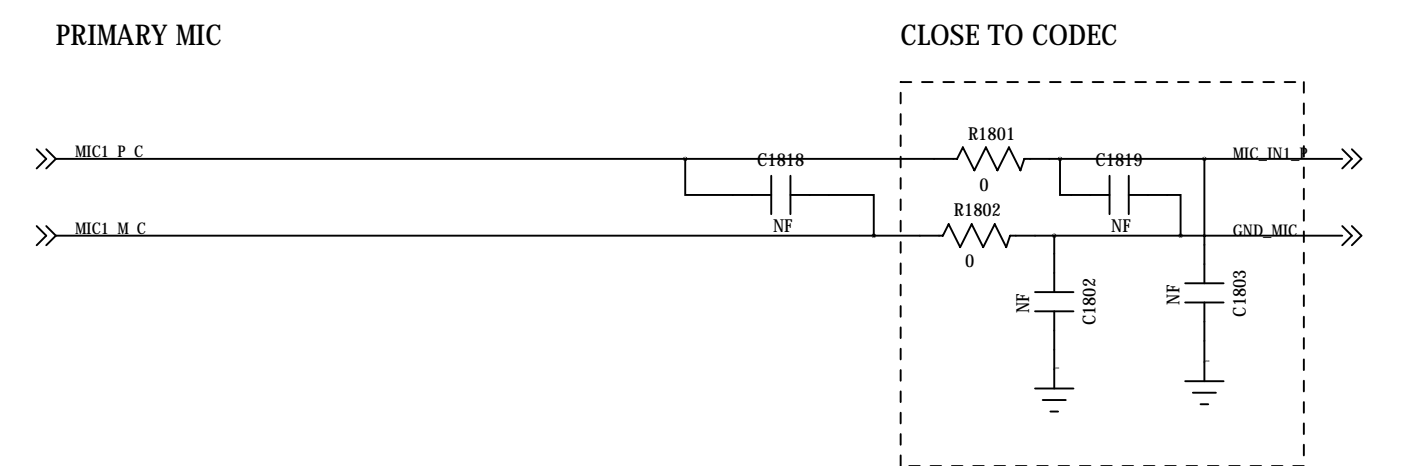
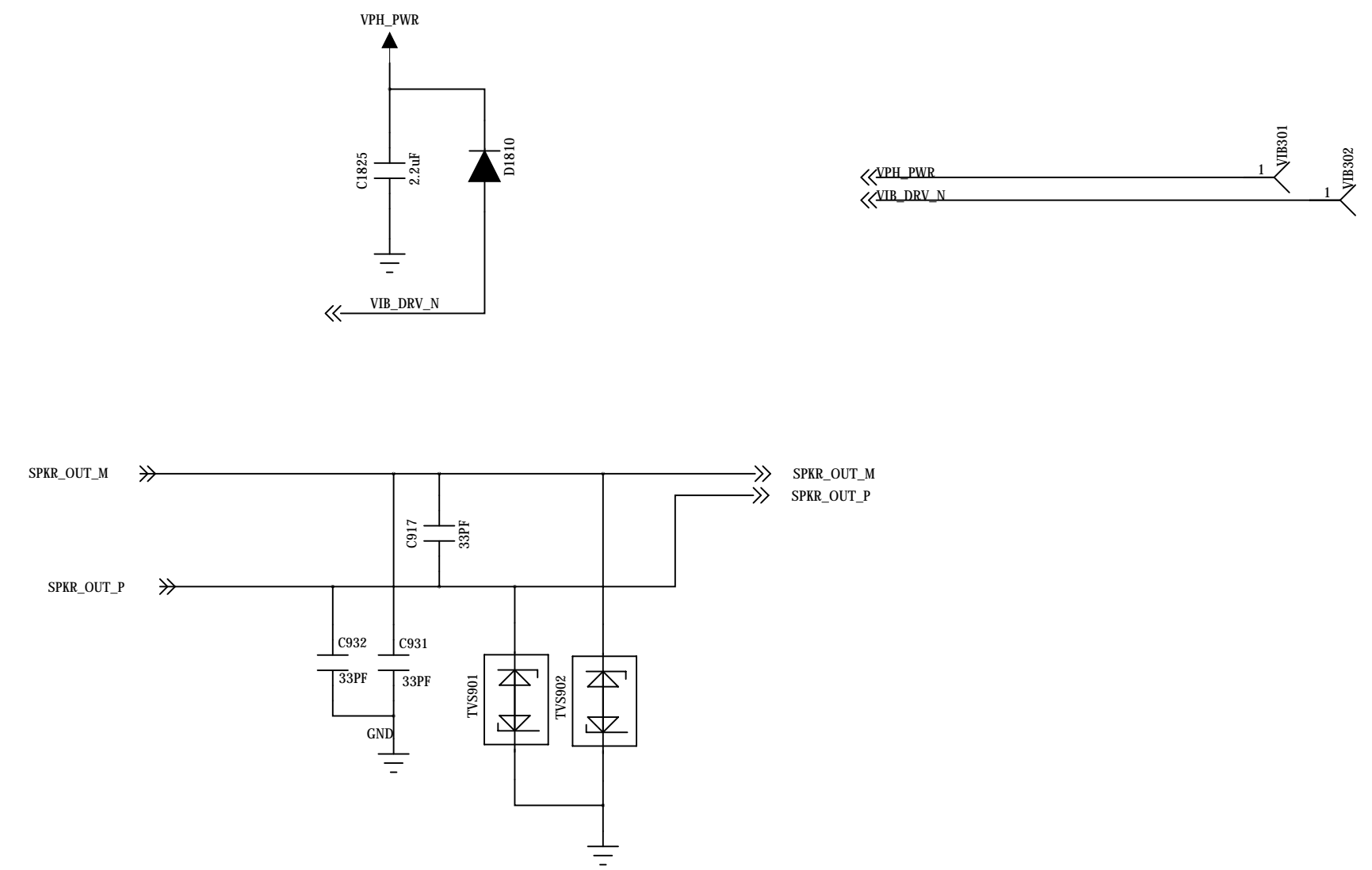
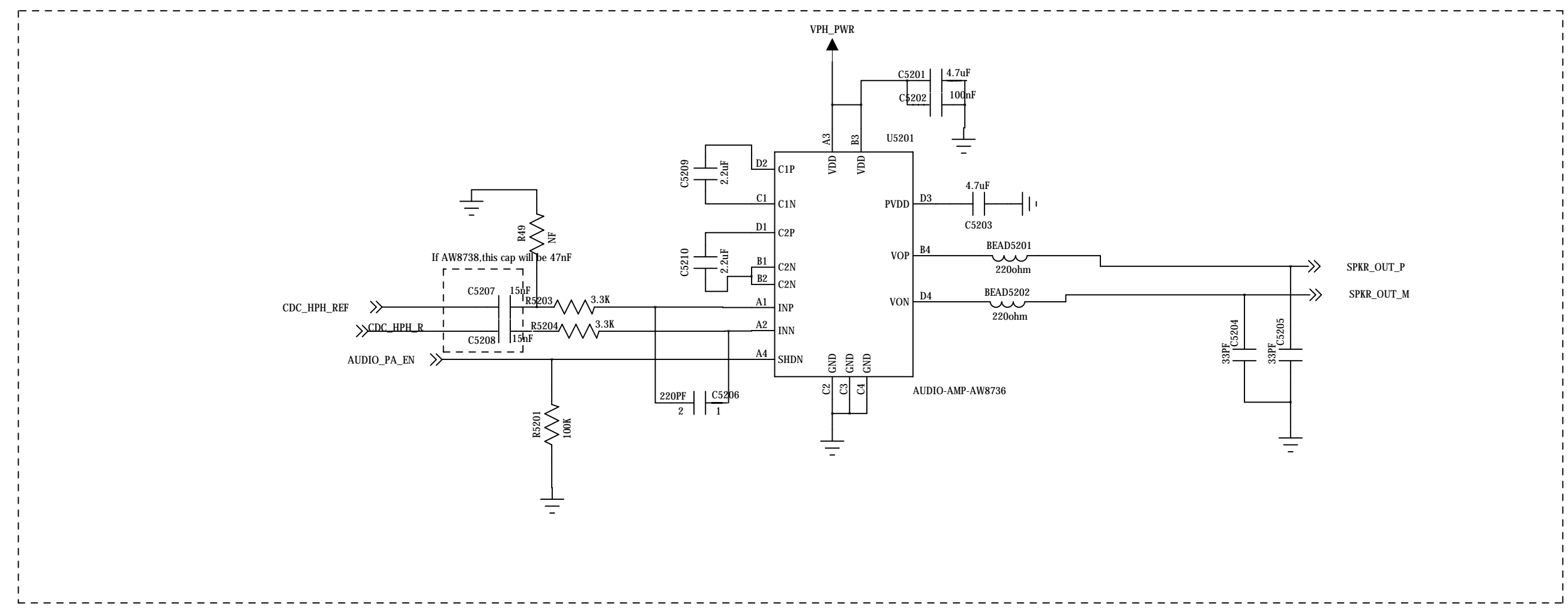
M-MIC+USB+RGB+SPK

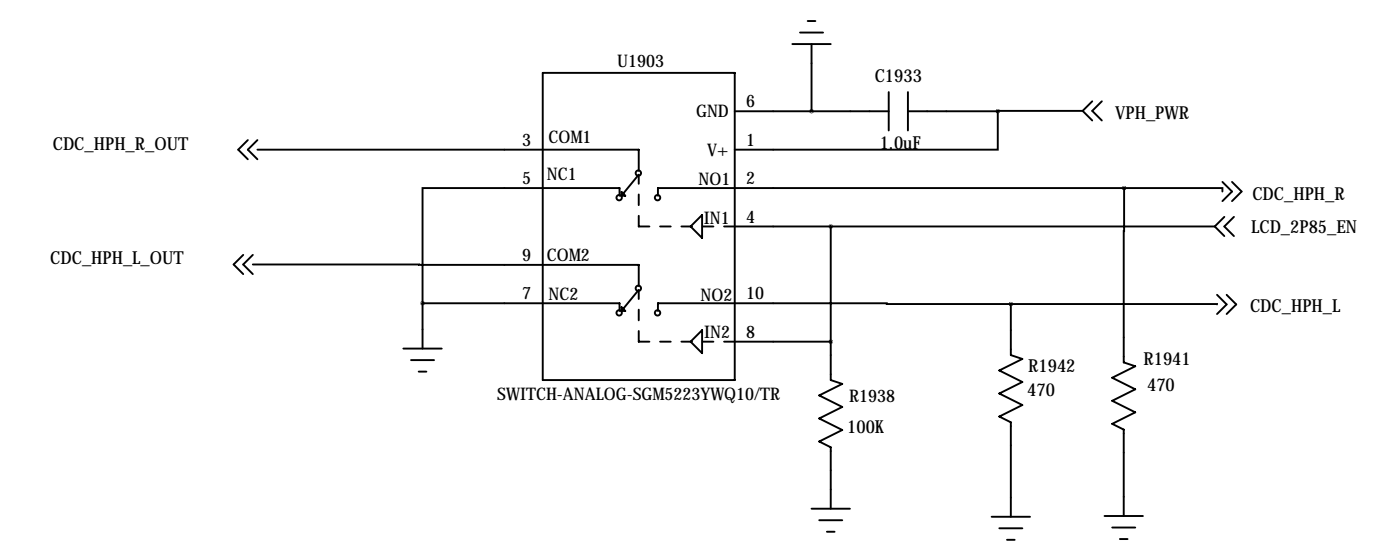
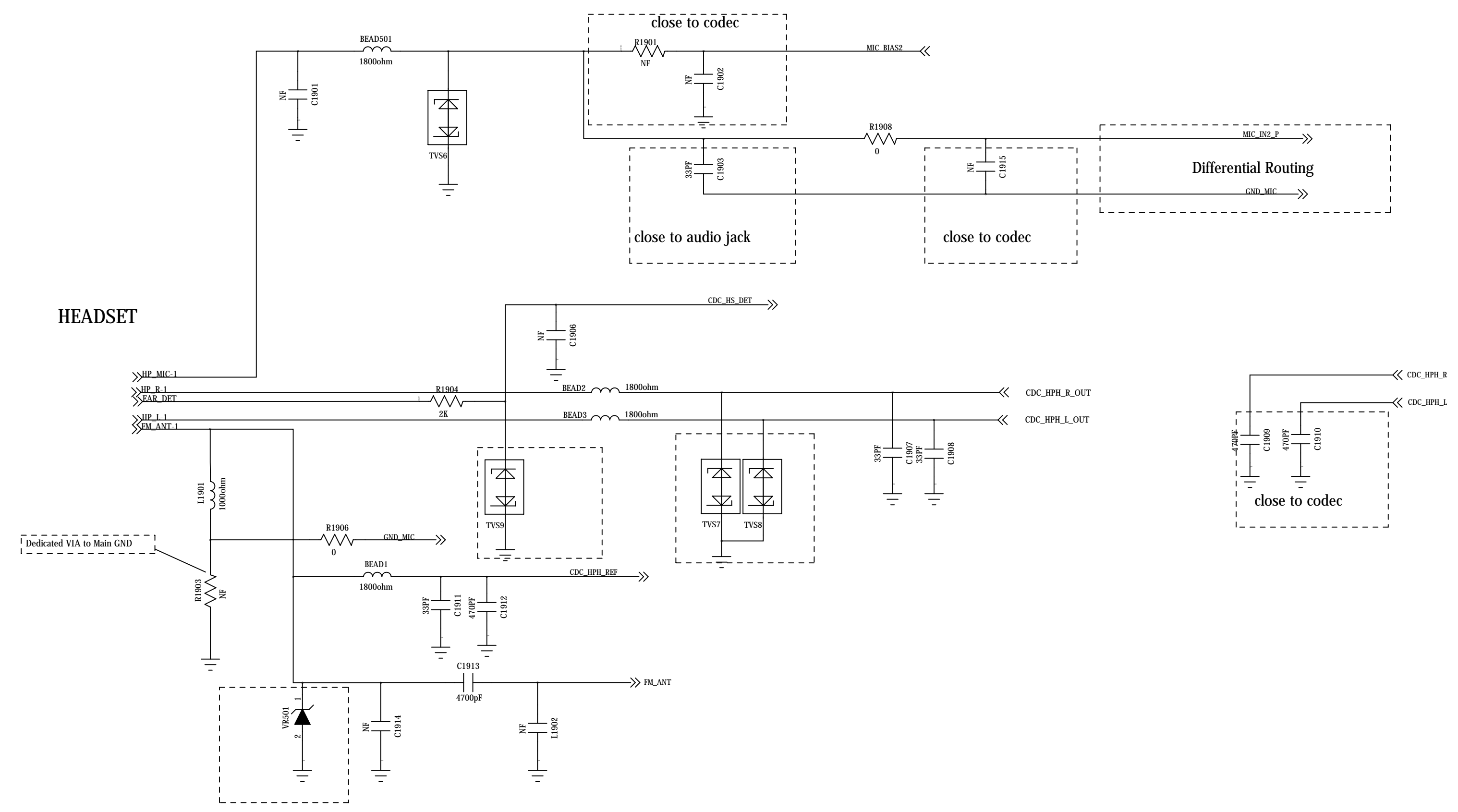
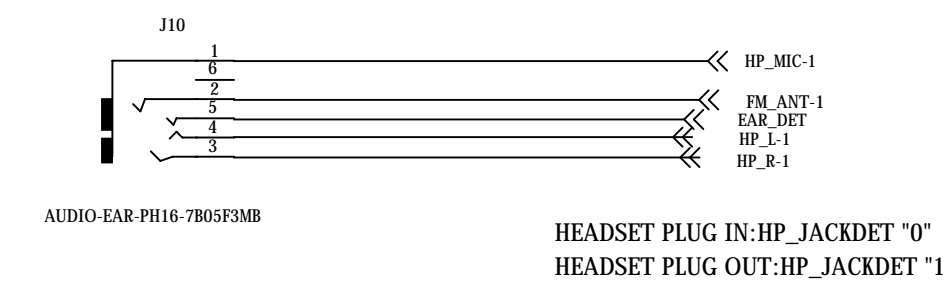


RGB

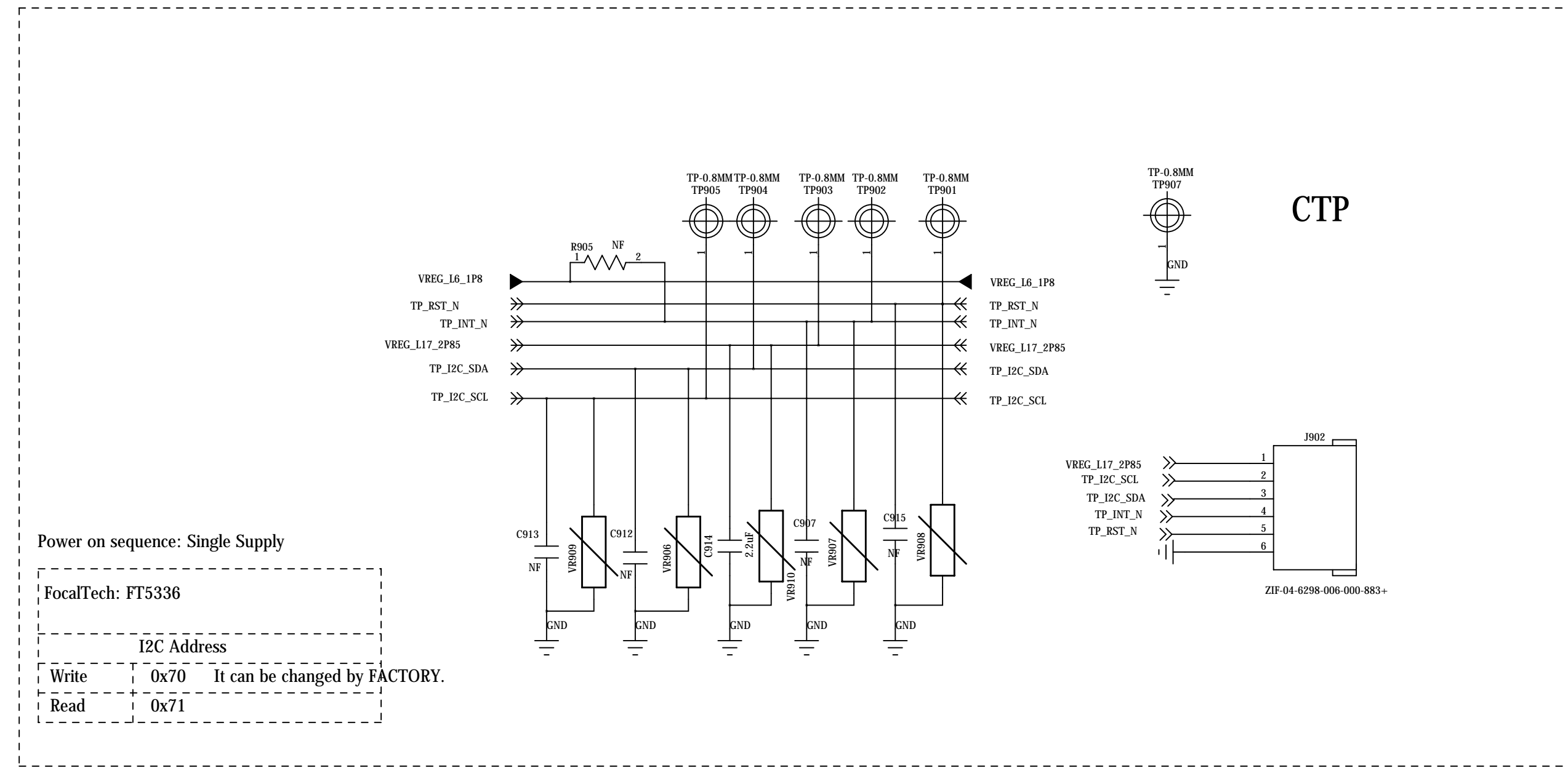
I2C Address	
Write	8B0x8A
Read	8B0x8B

Power on sequence: can be applied in any order

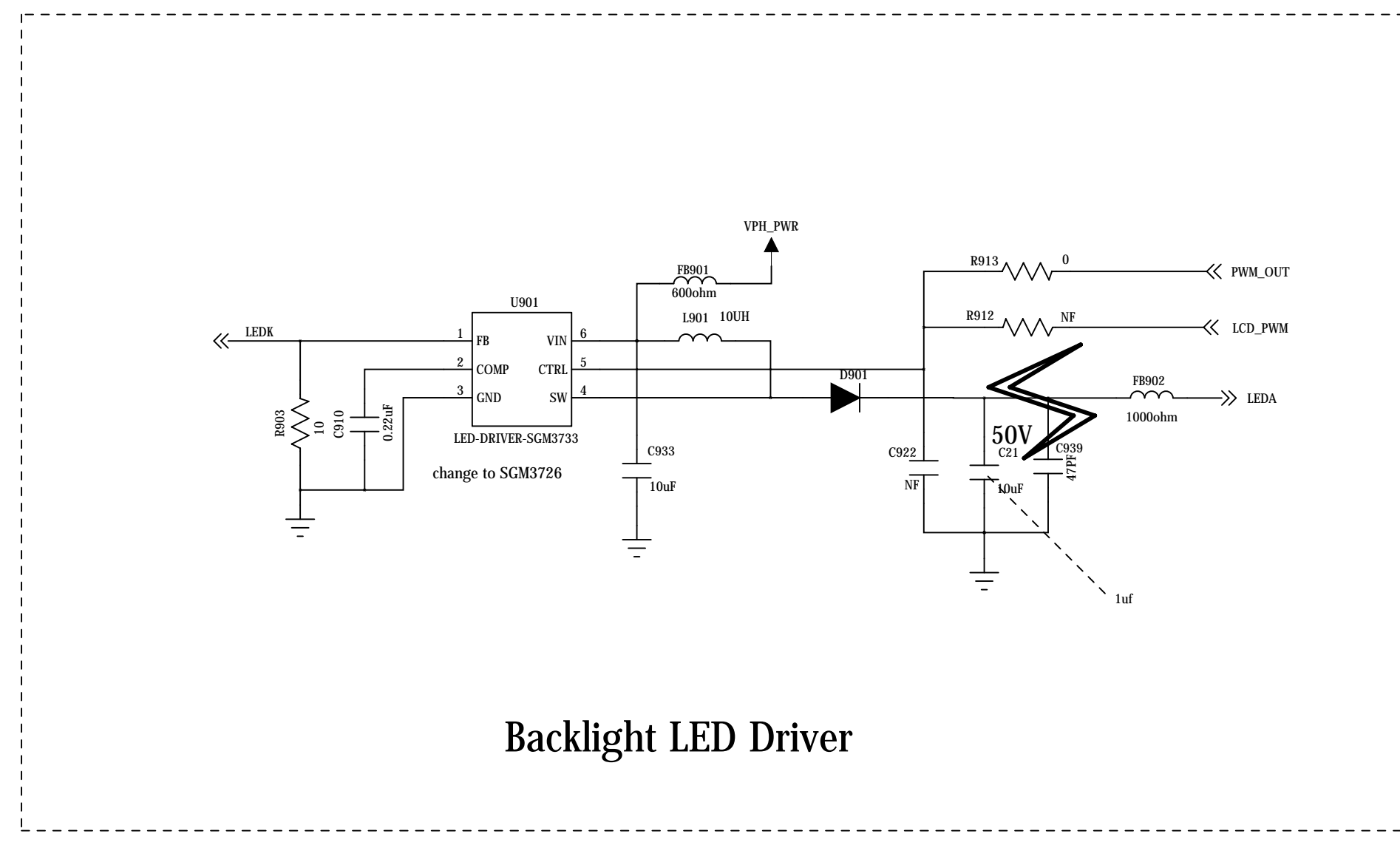
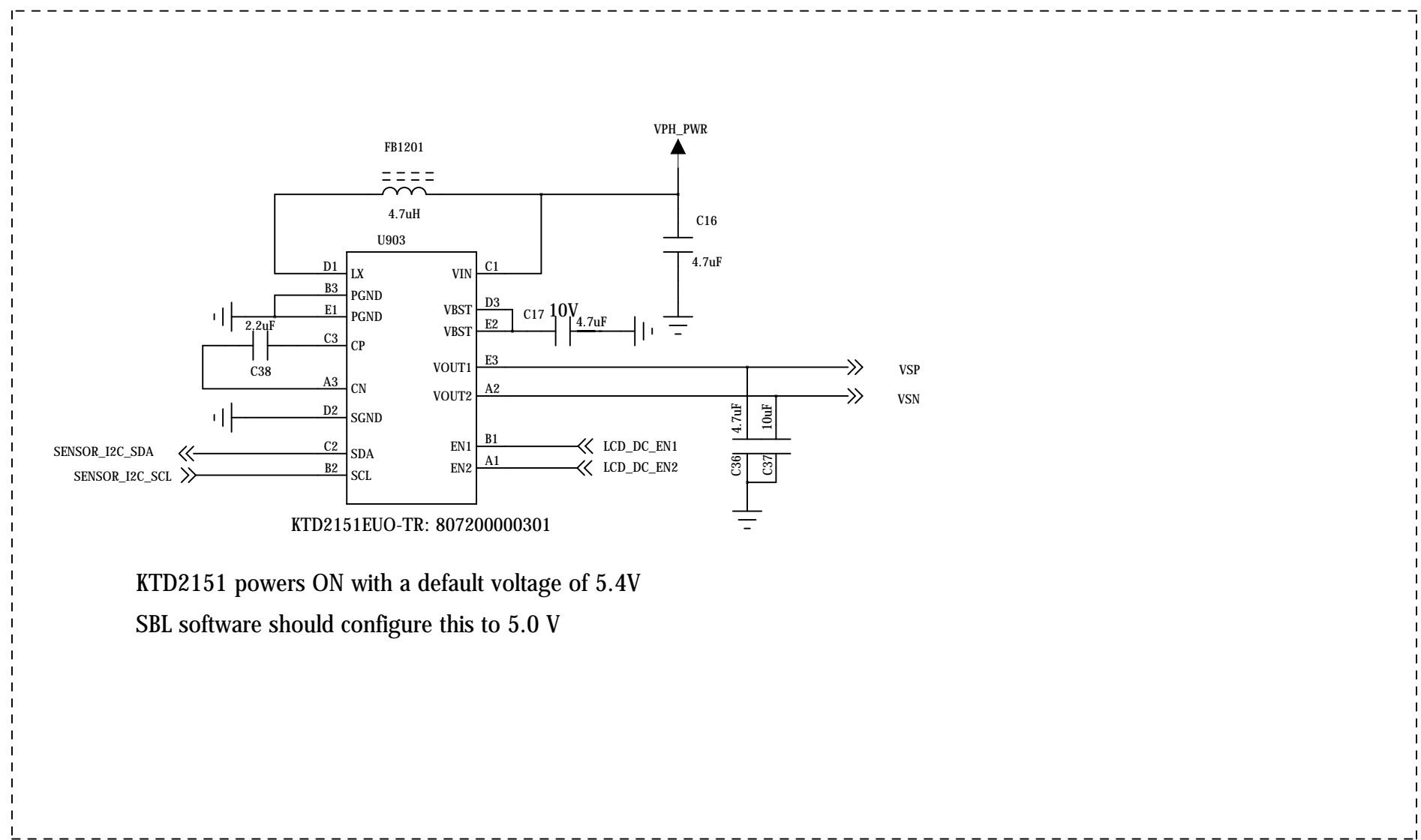
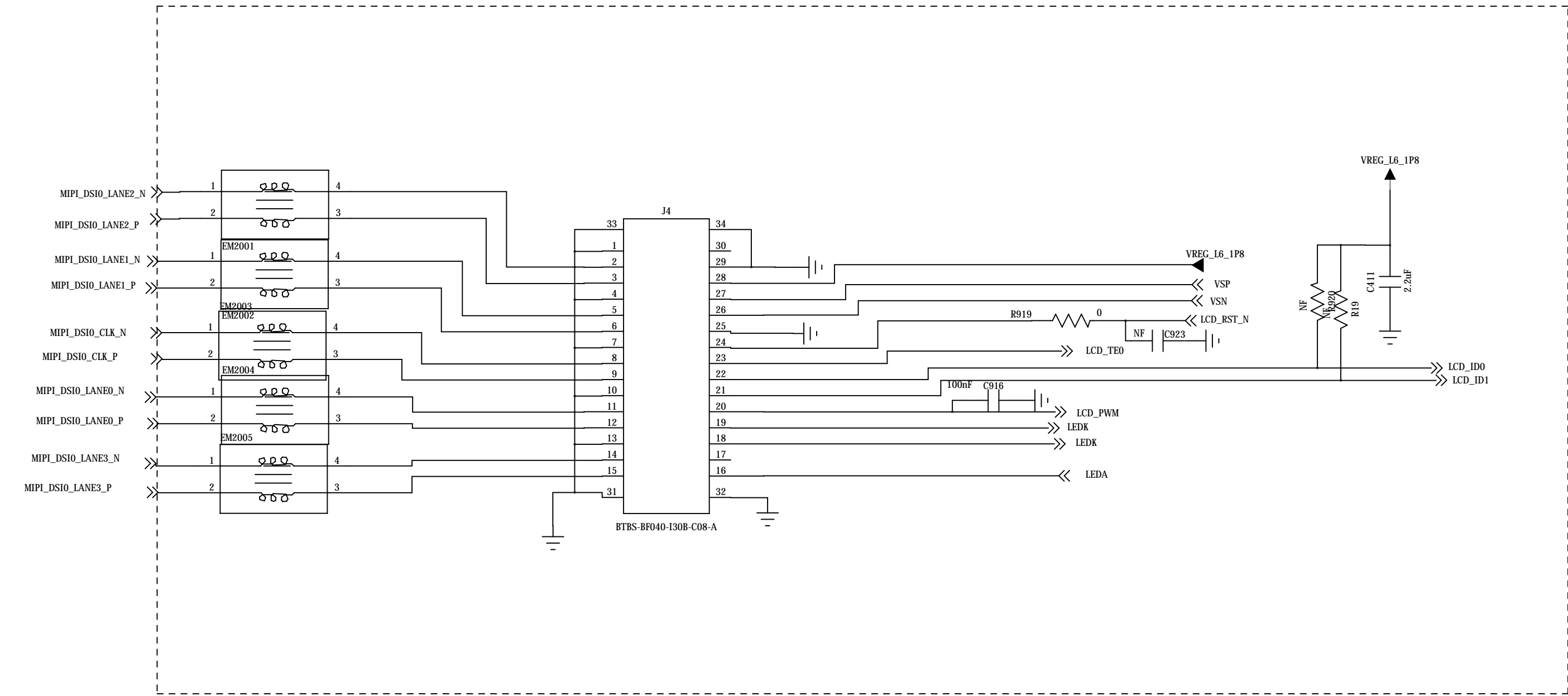




IN=0, COM Connected to NC;
IN=1, COM Connected to NO;

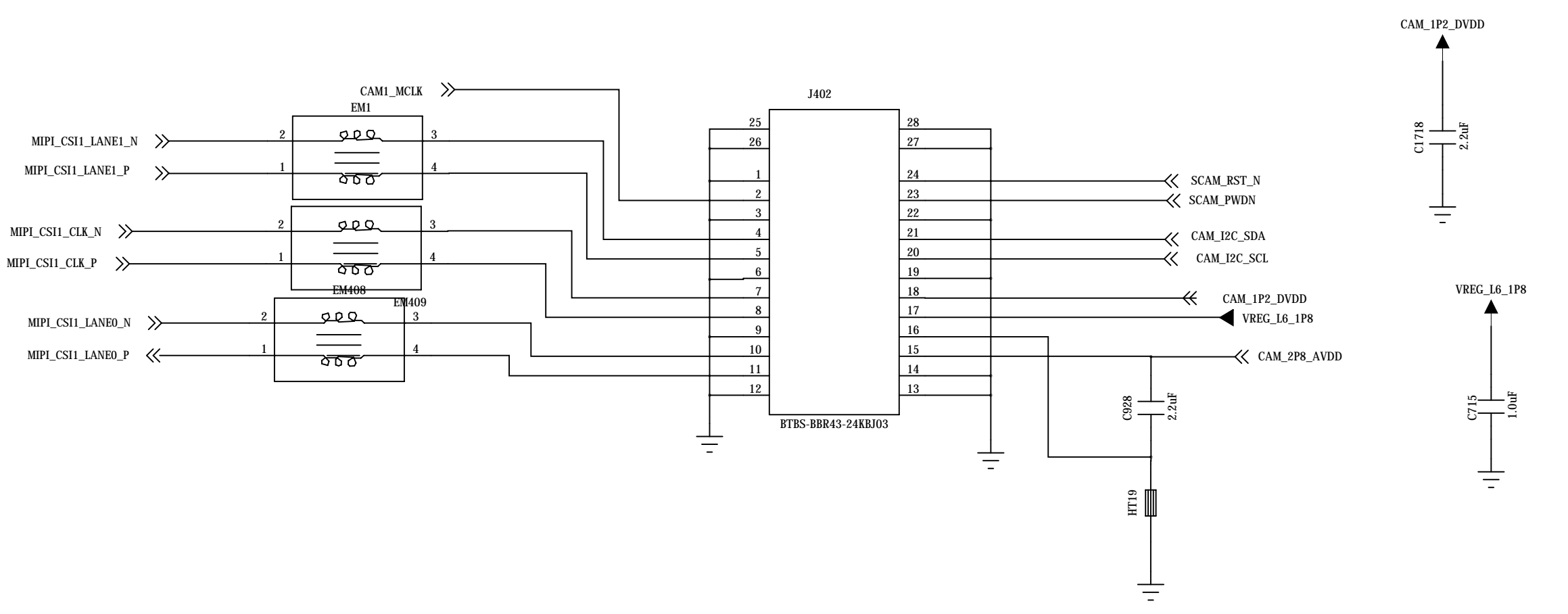


LCD
5.0" FHD



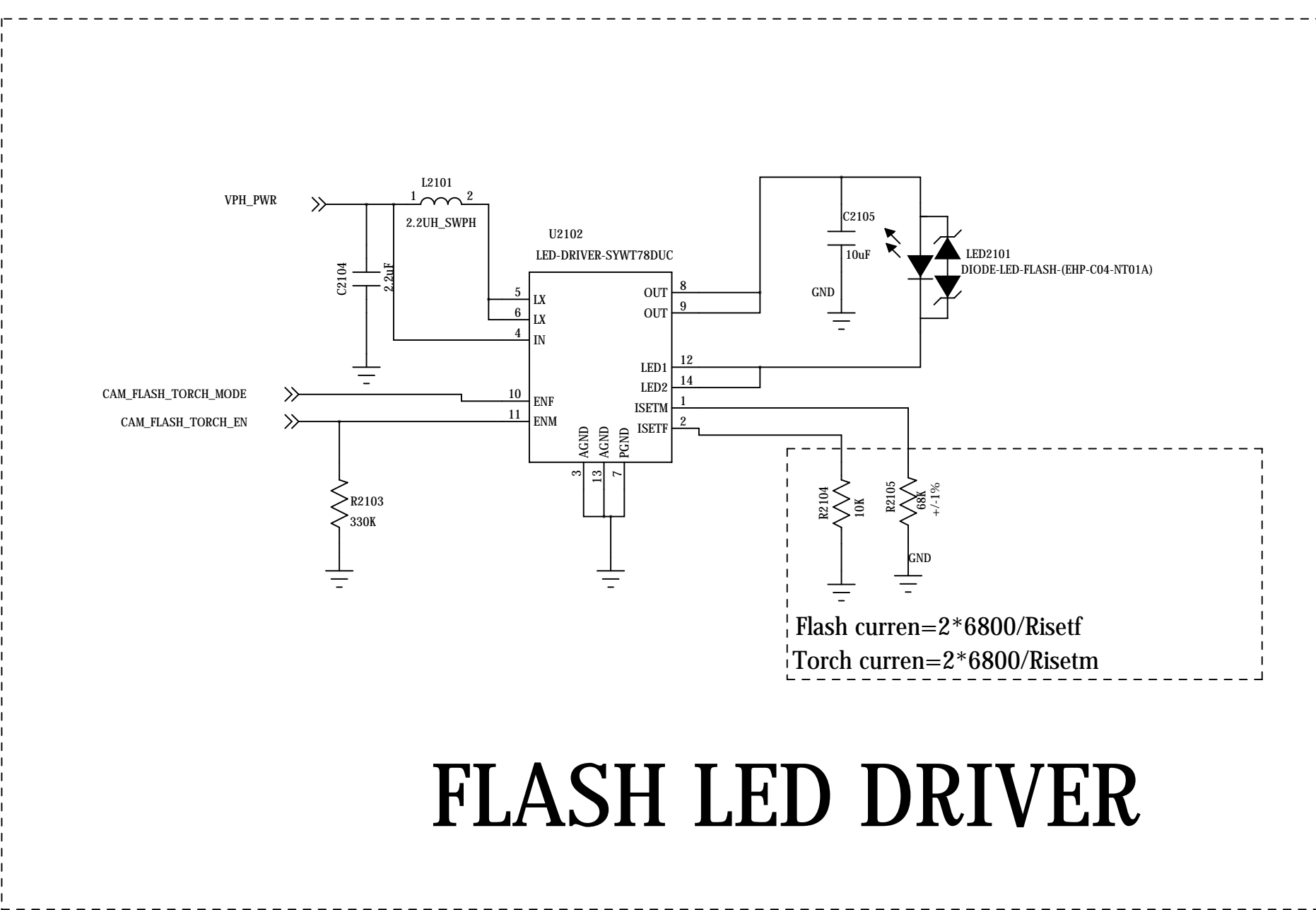
PIN	
1	GND
2	MCLK
3	GND
4	MDN1
5	MDP1
6	GND
7	MCN
8	MCP
9	GND
10	MDNO
11	MDPO
12	GND
13	GND
14	GND
15	AVDD 2.8V
16	GND
17	DOVDD 1.8V
18	DVDD 1.2V
19	GND
20	SCL
21	SDA
22	GND
23	PWDN
24	RESET

Sub Camera



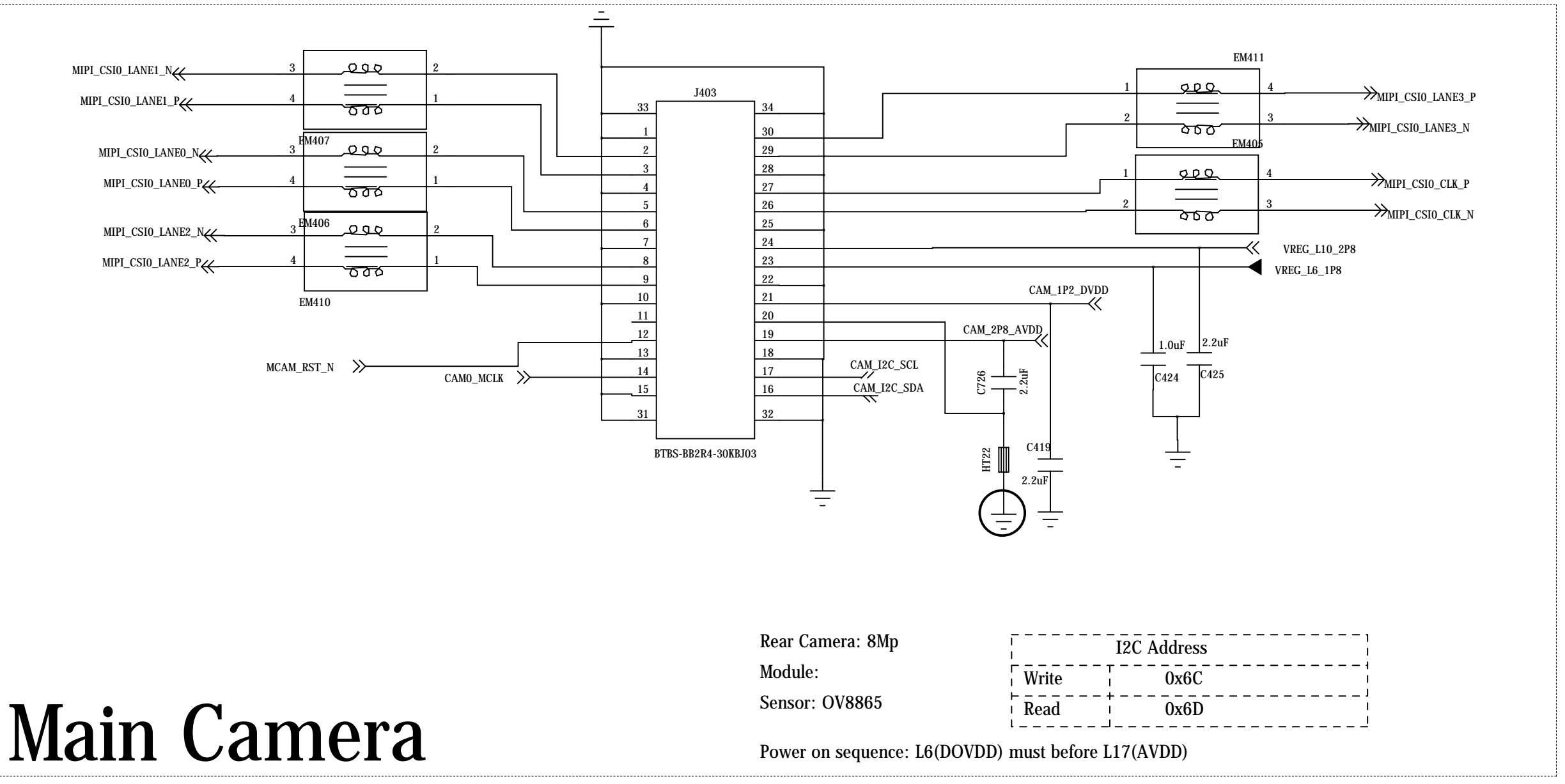
FRONT_camera

Main Camera / Sub Camera share power domain design should double check the voltage level is compatible



FLASH LED DRIVER

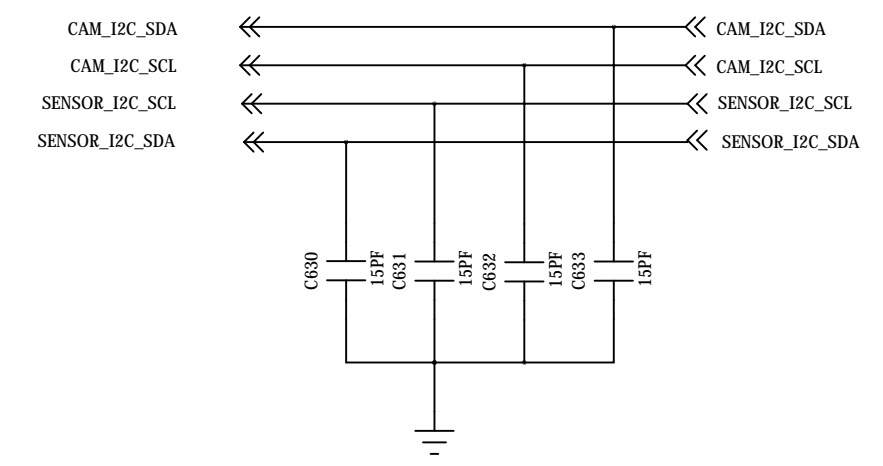
Main Camera / Sub Camera share power domain design should double check the voltage level is compatible

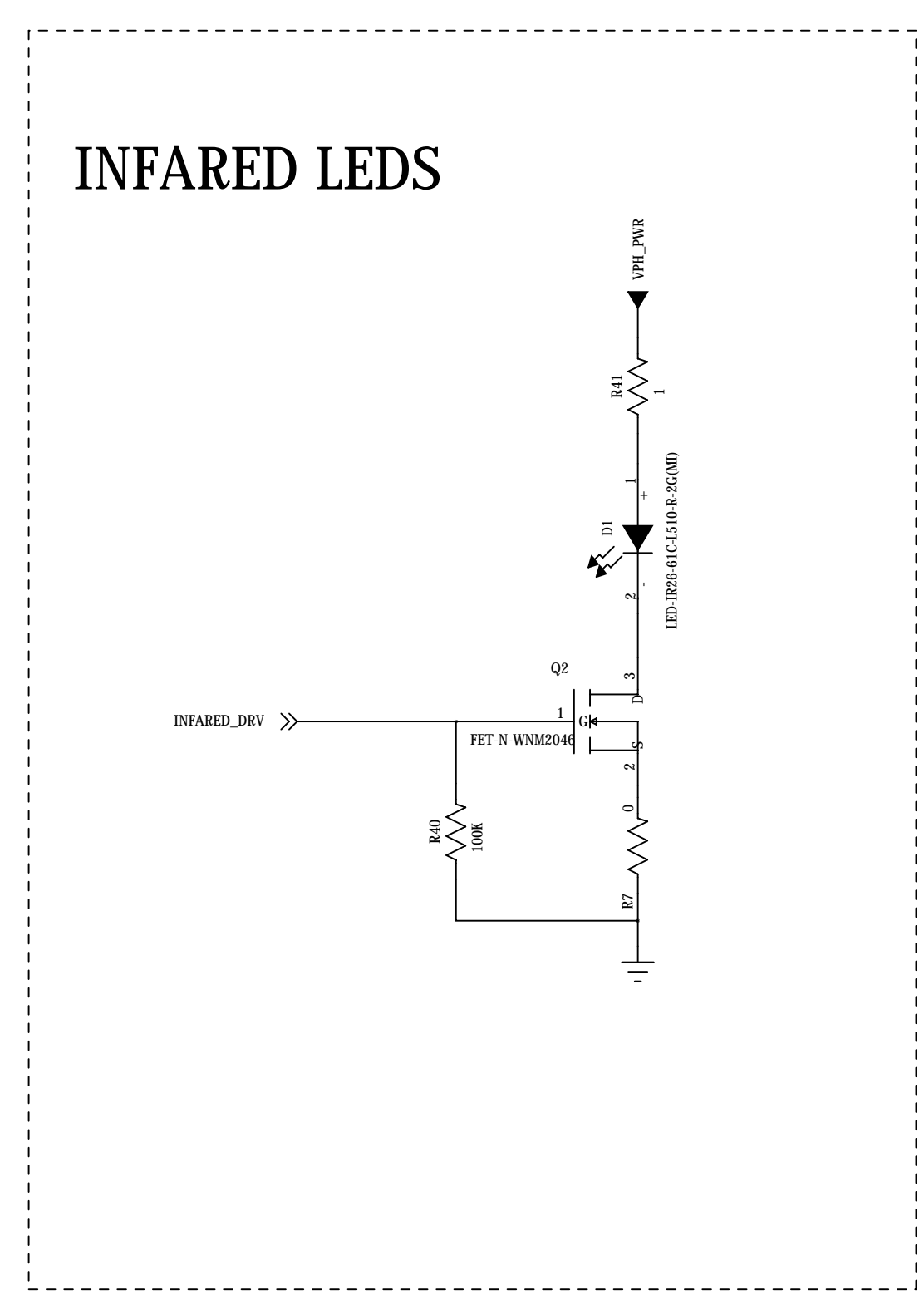
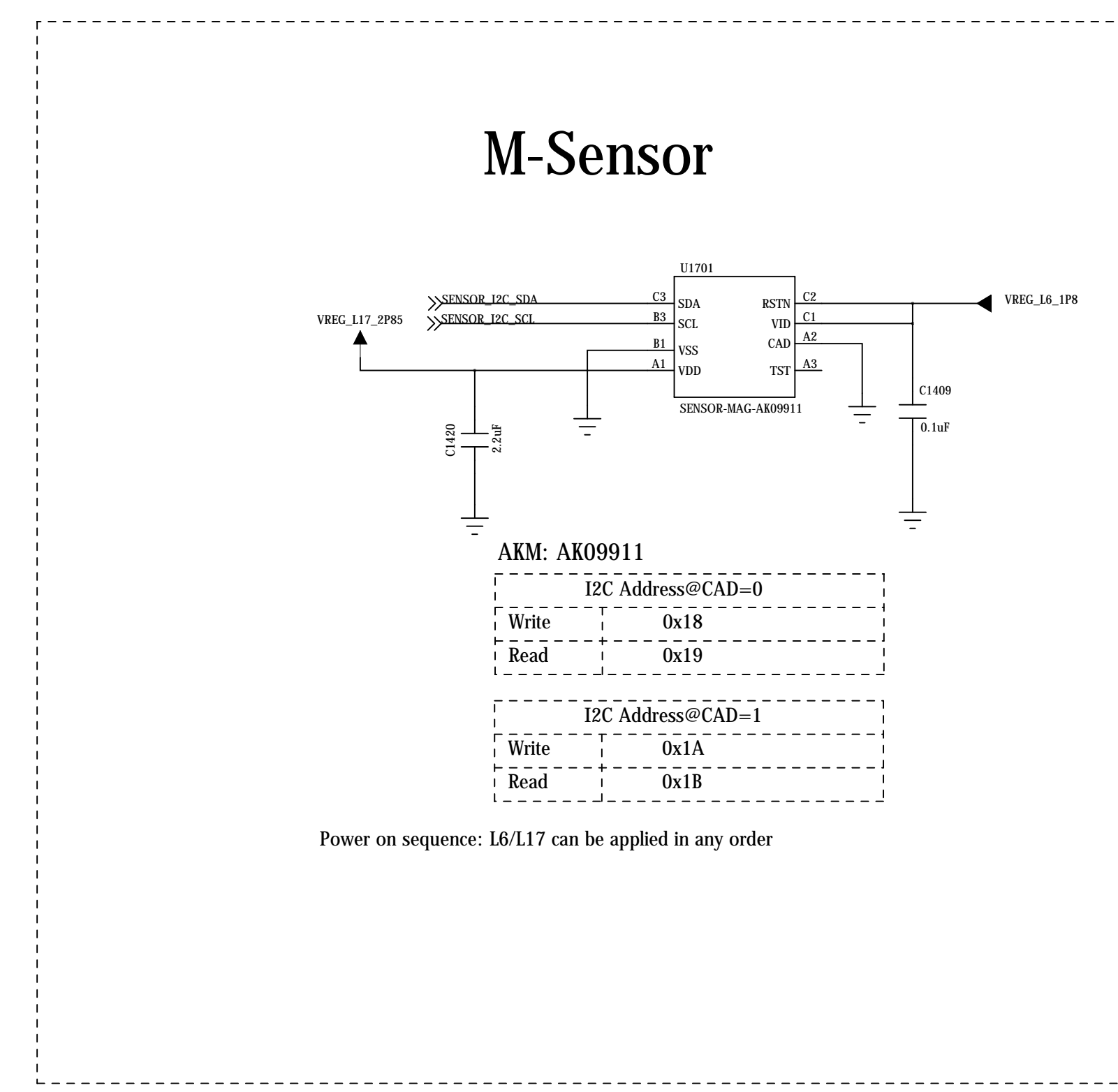
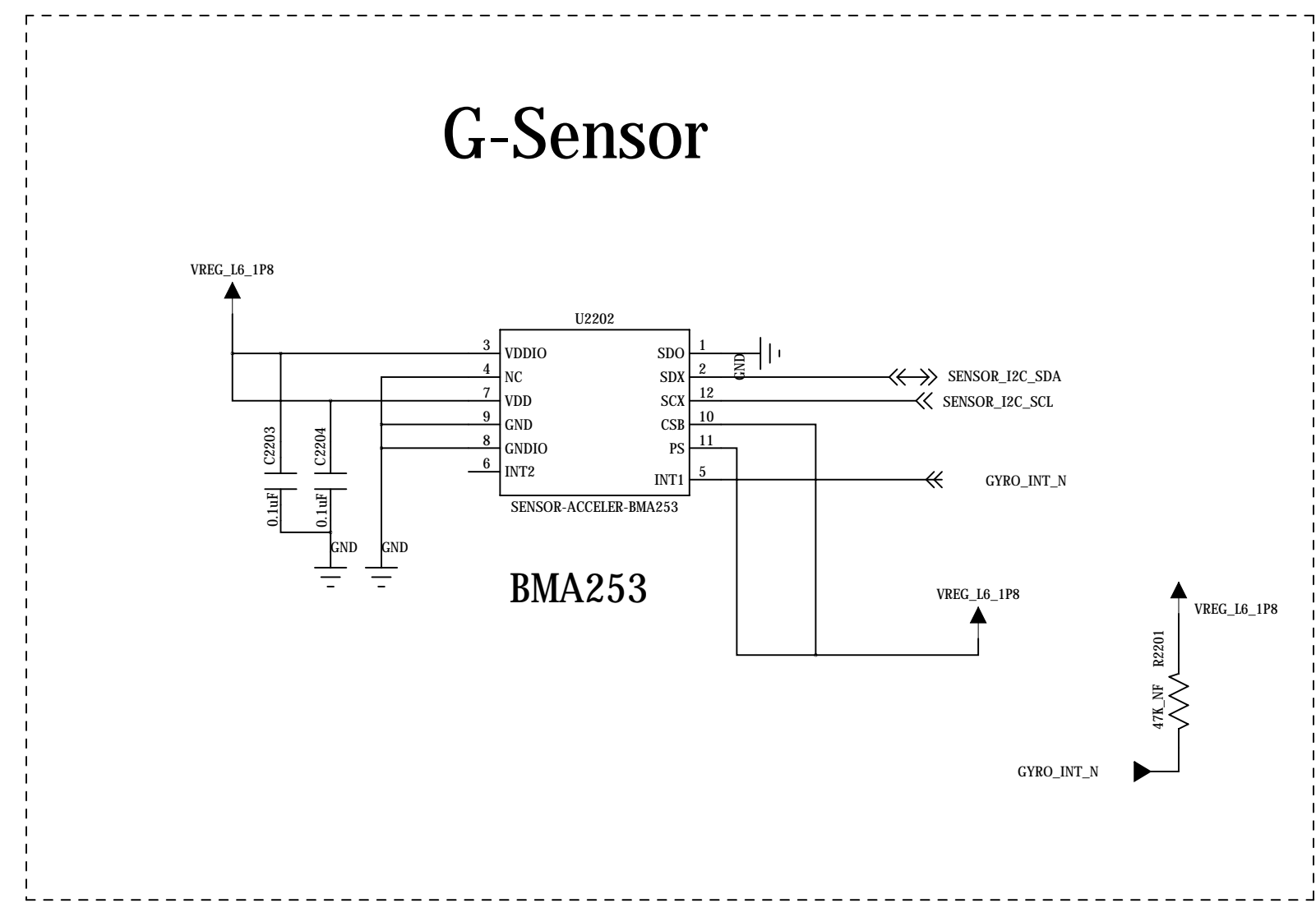
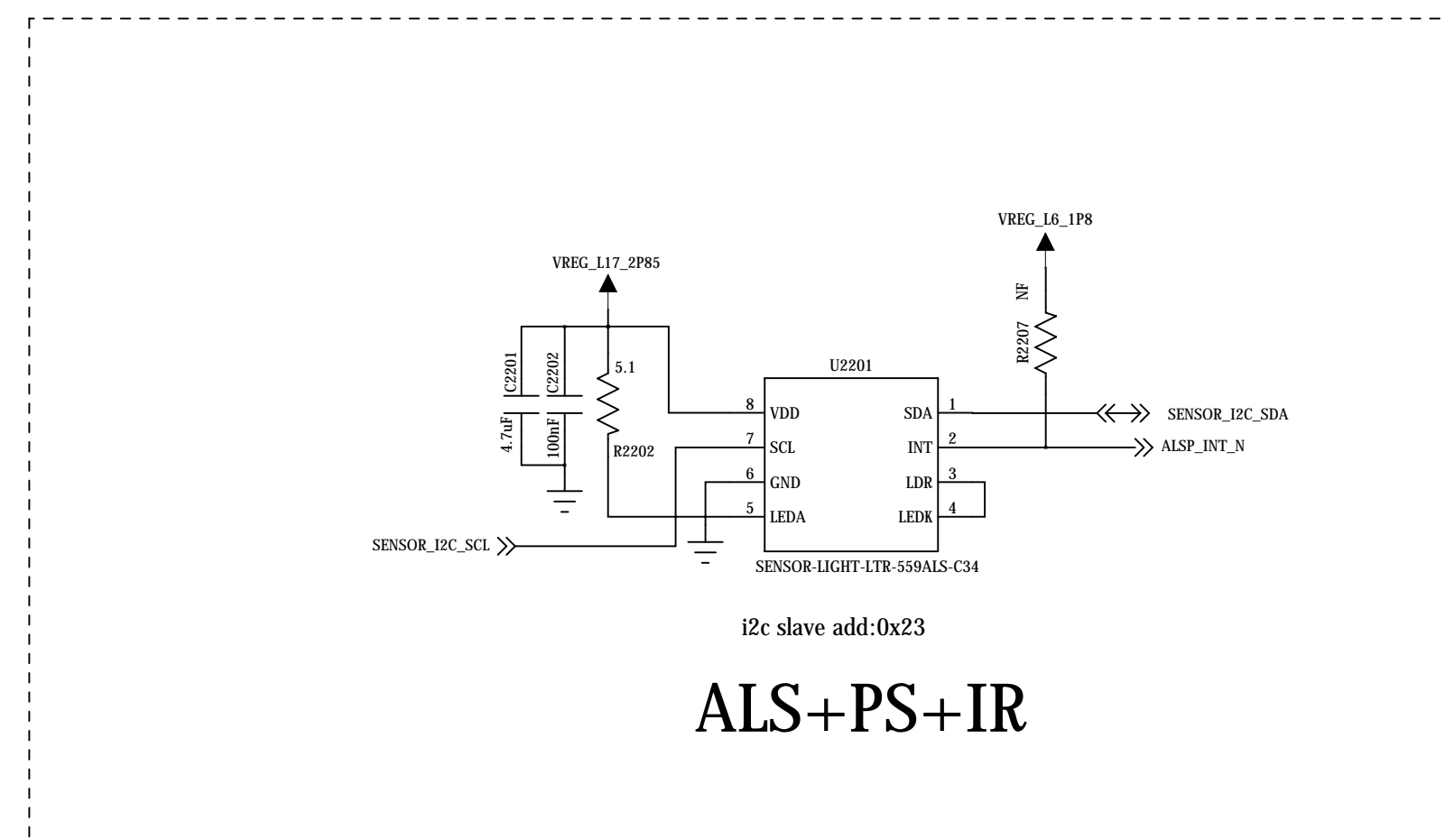


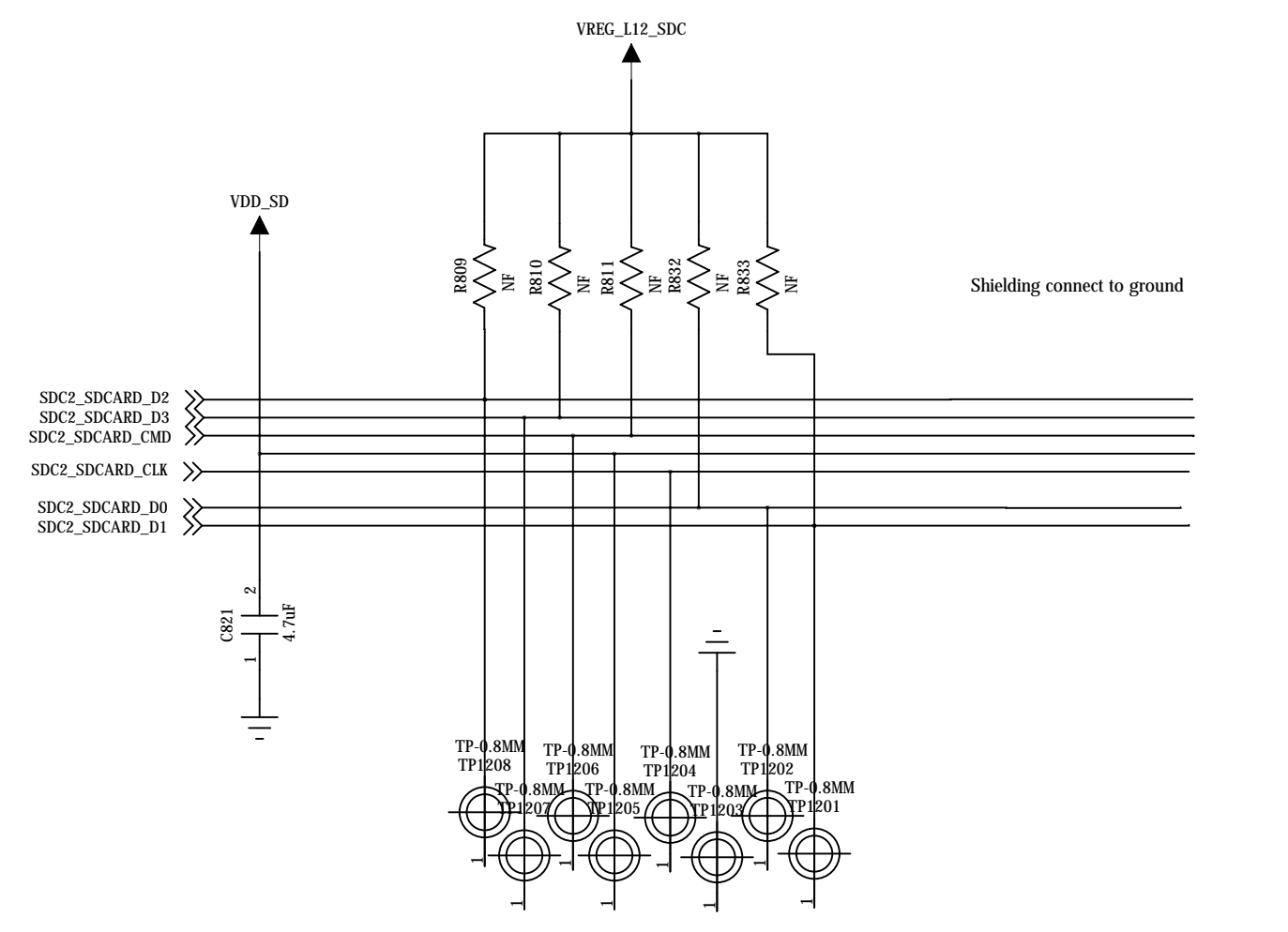
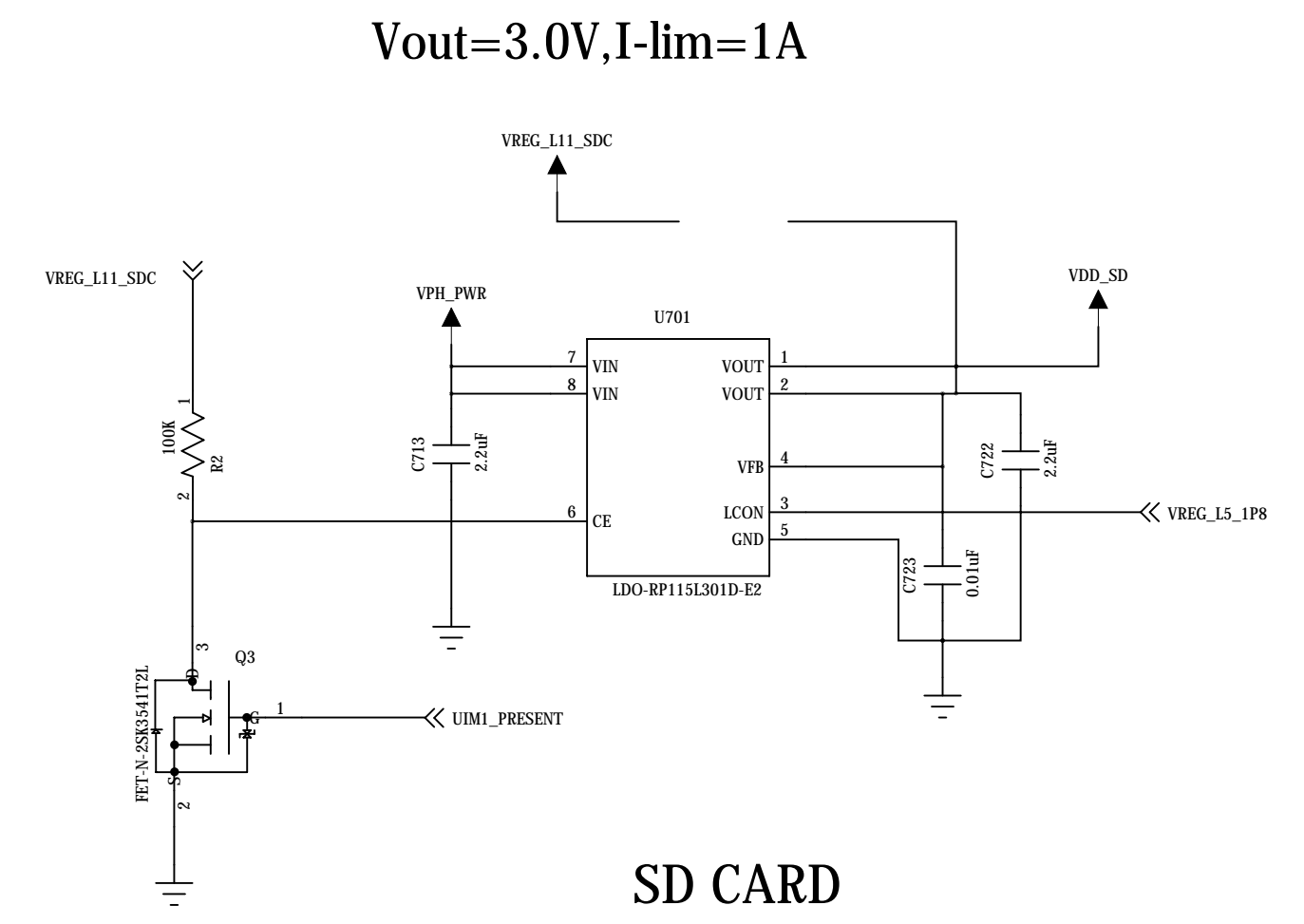
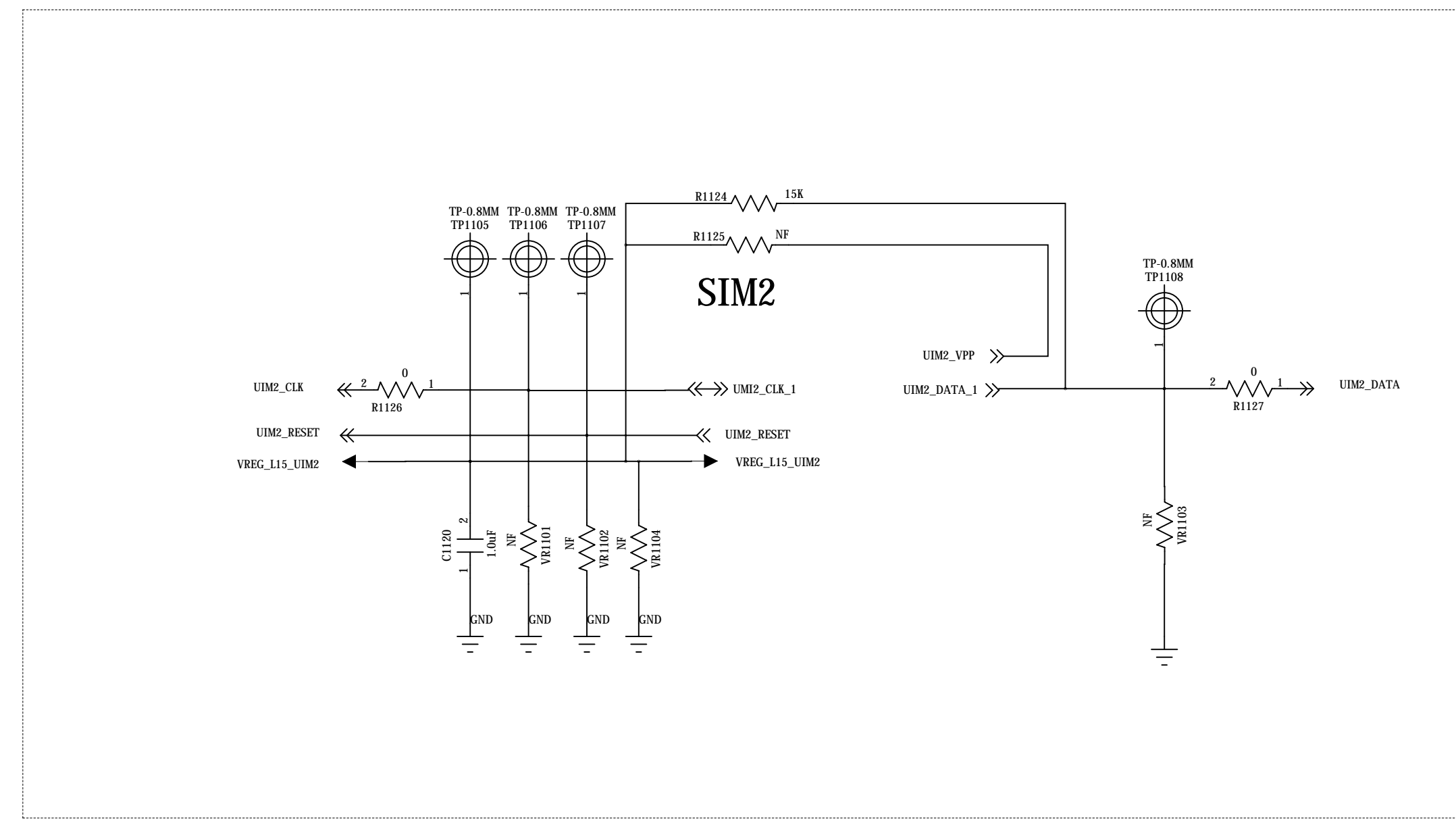
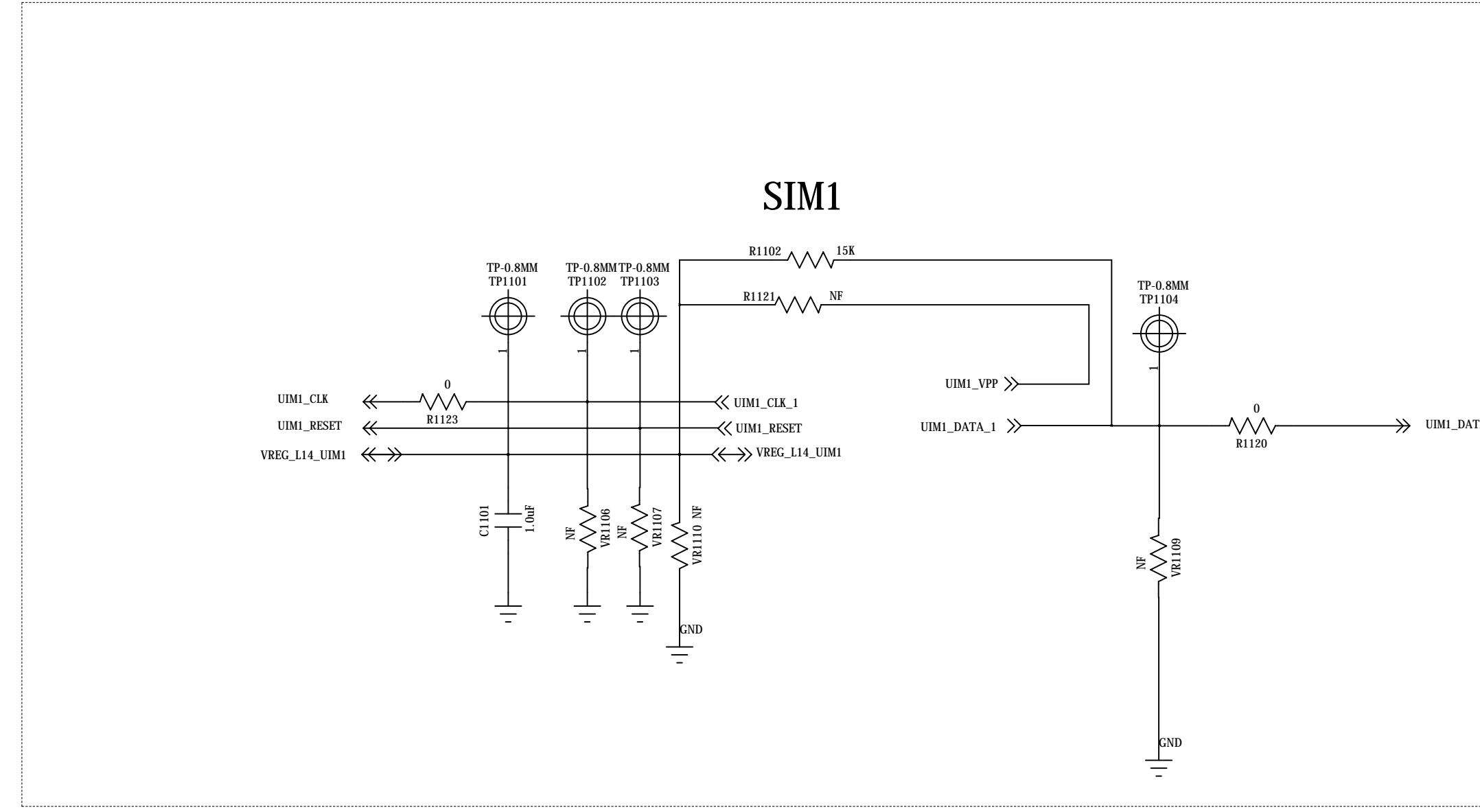
Main Camera

Rear Camera: 8Mp
Module:
Sensor: OV8865
Power on sequence: L6(DOVDD) must before L17(AVDD)

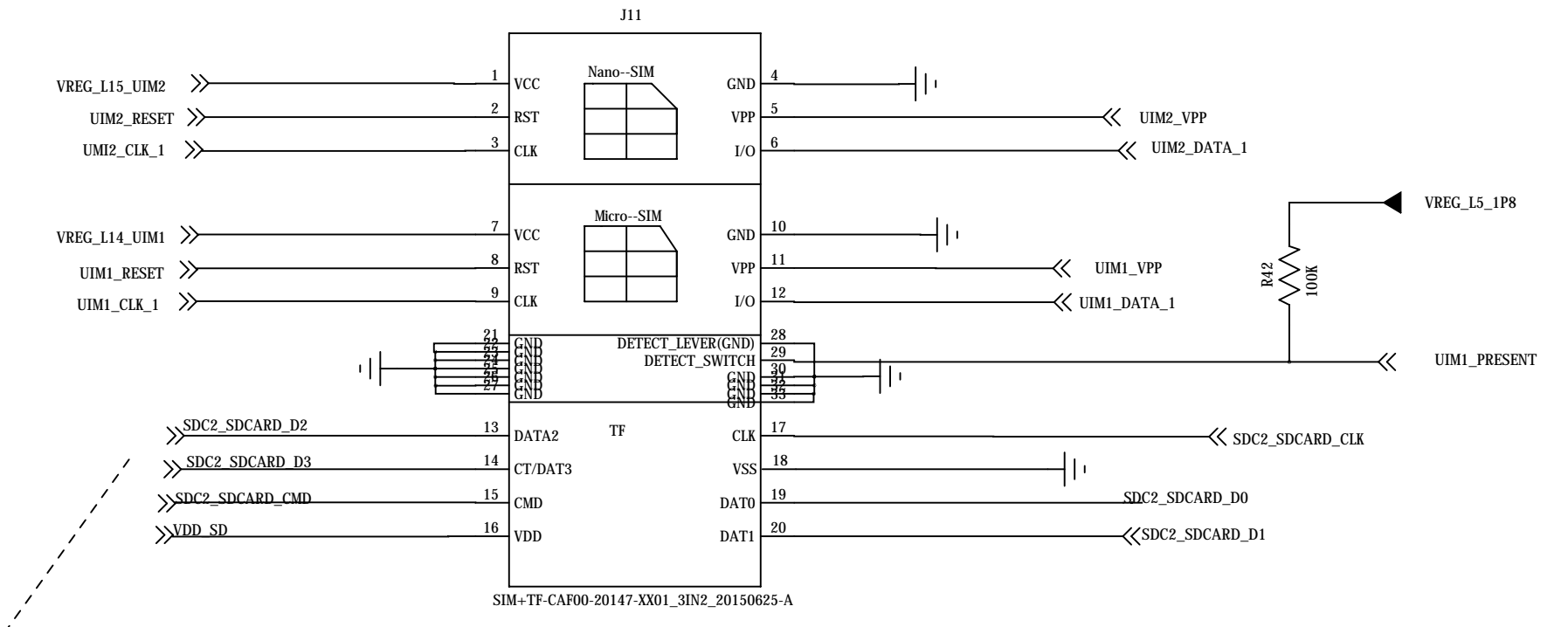
I2C Address	
Write	0x6C
Read	0x6D







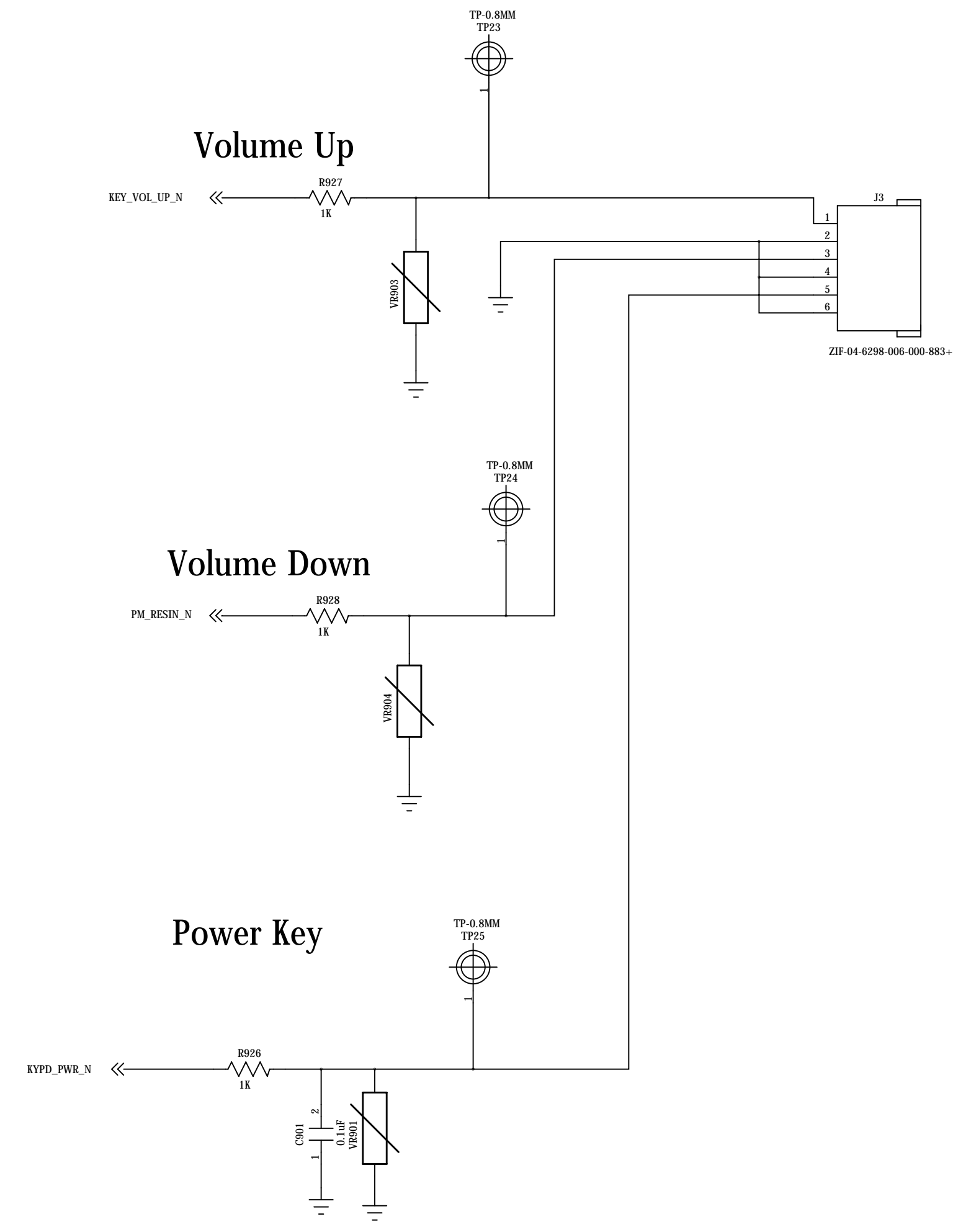
This int should give to GPIO38/GPIO56/GPIO60

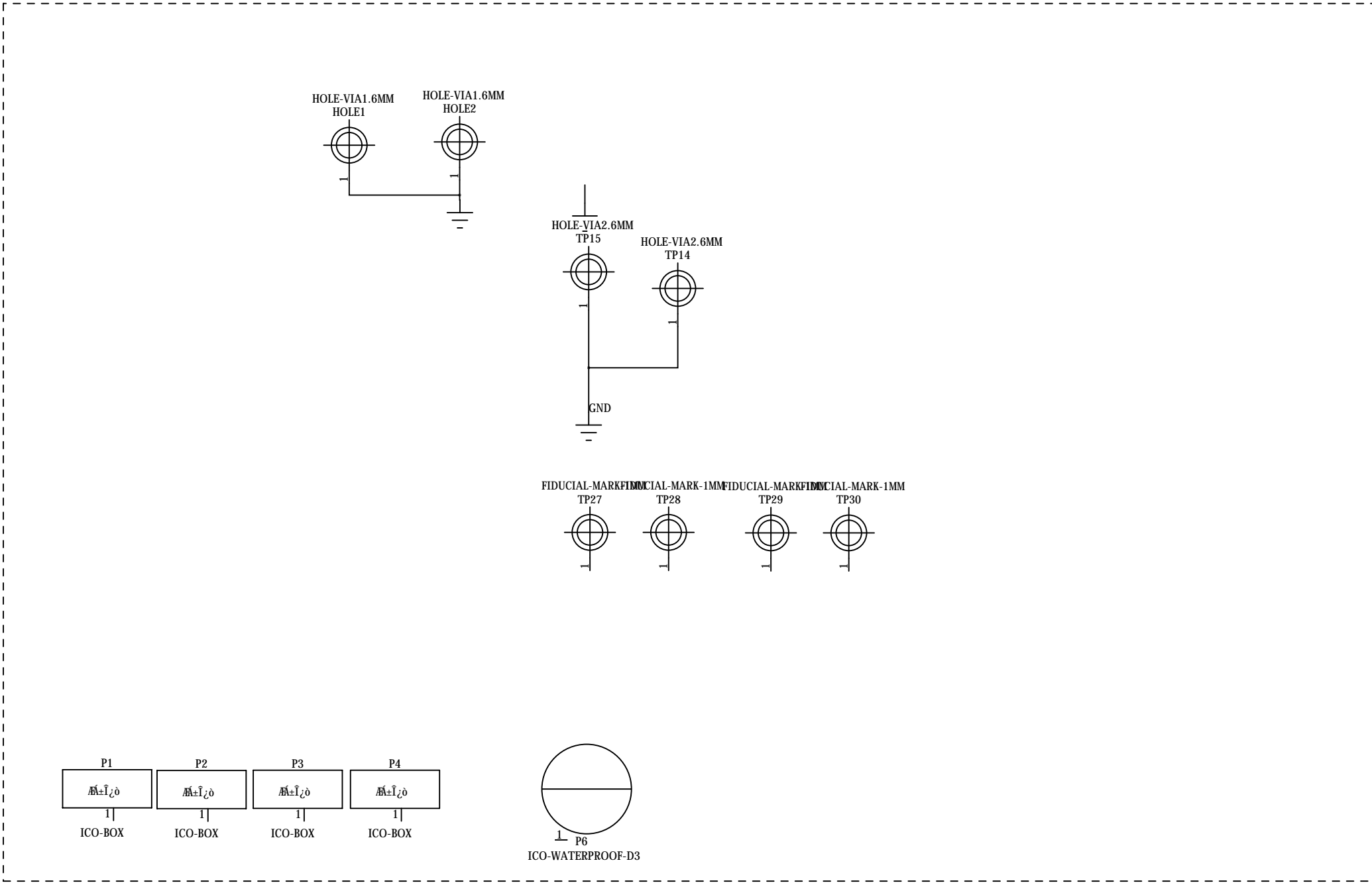
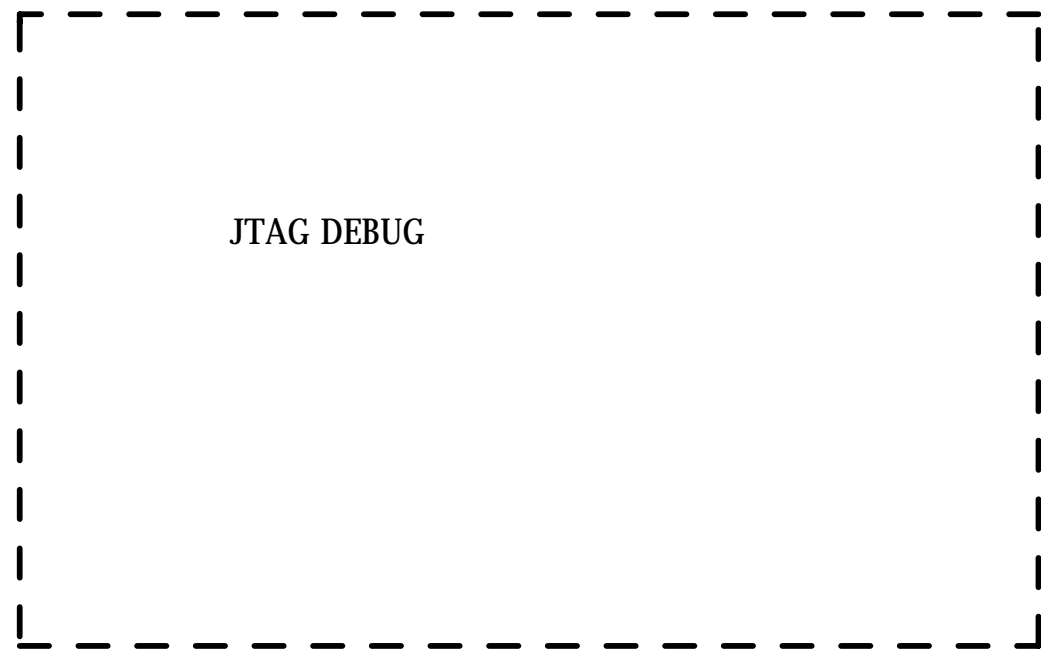
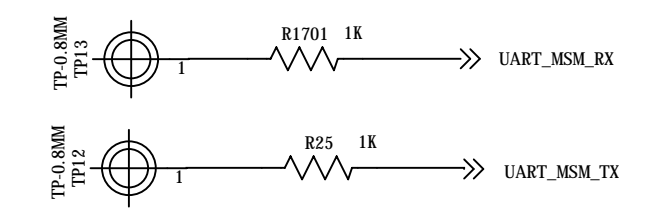
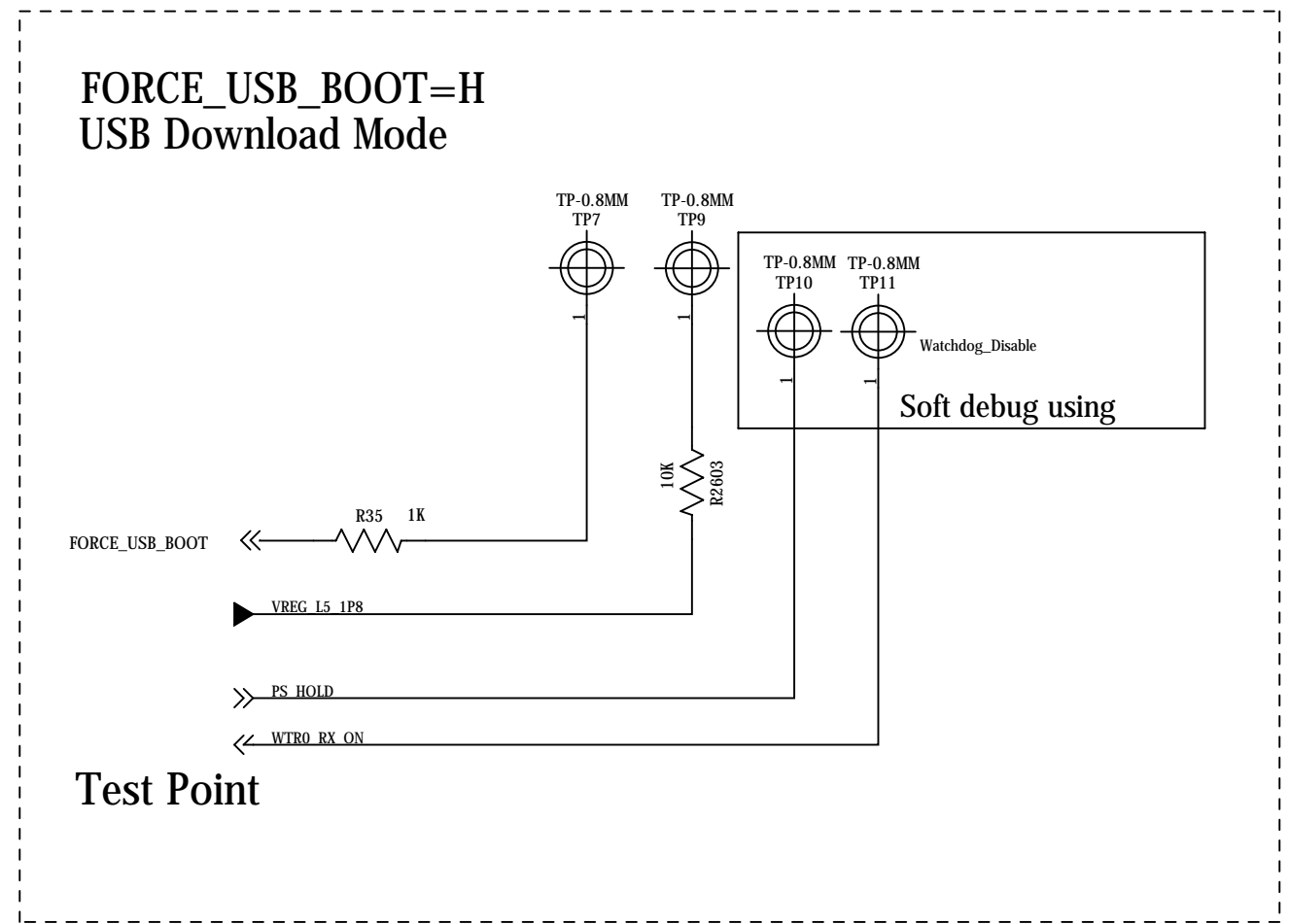


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Name		
Date:	Sheet	of

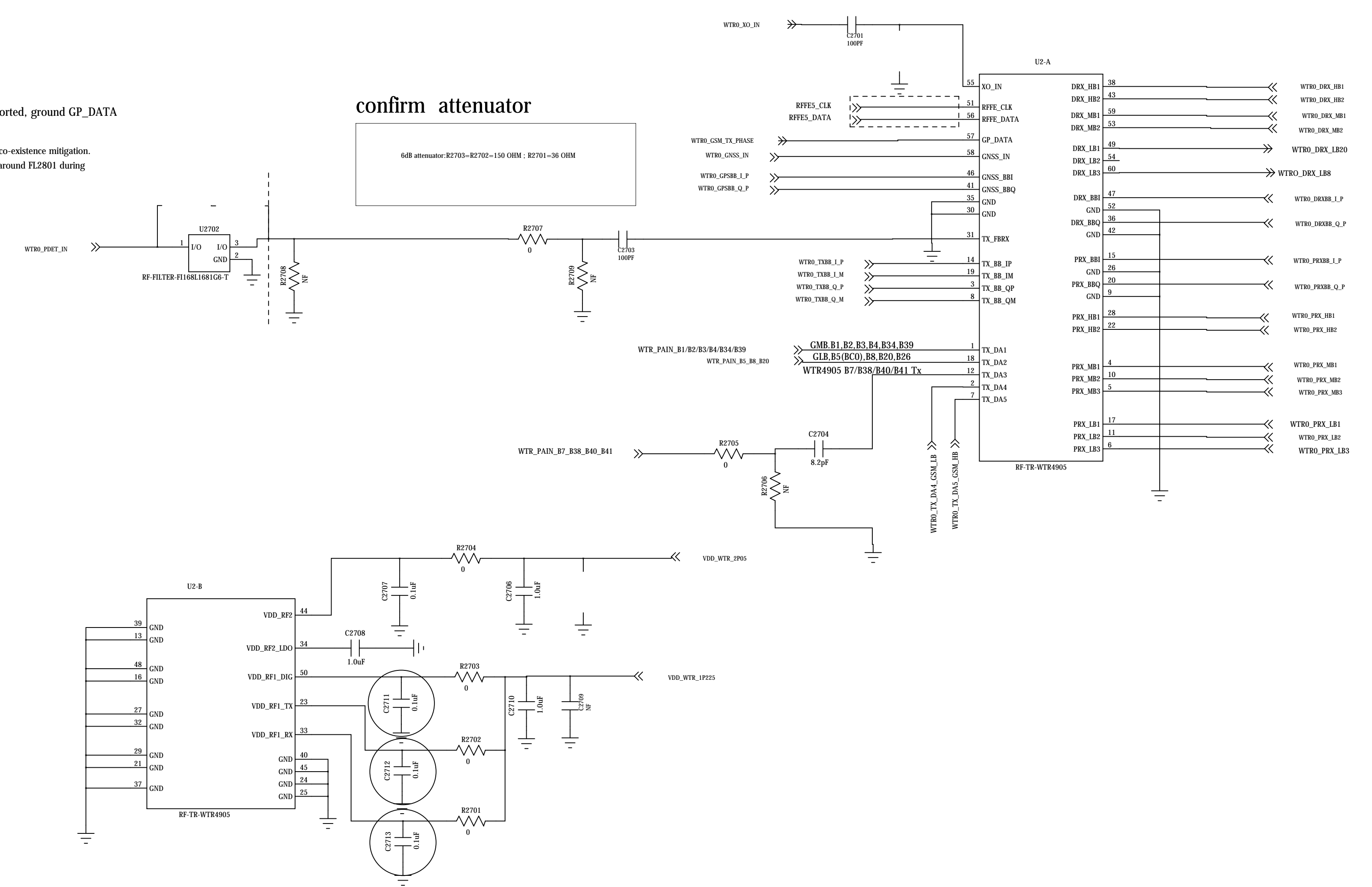


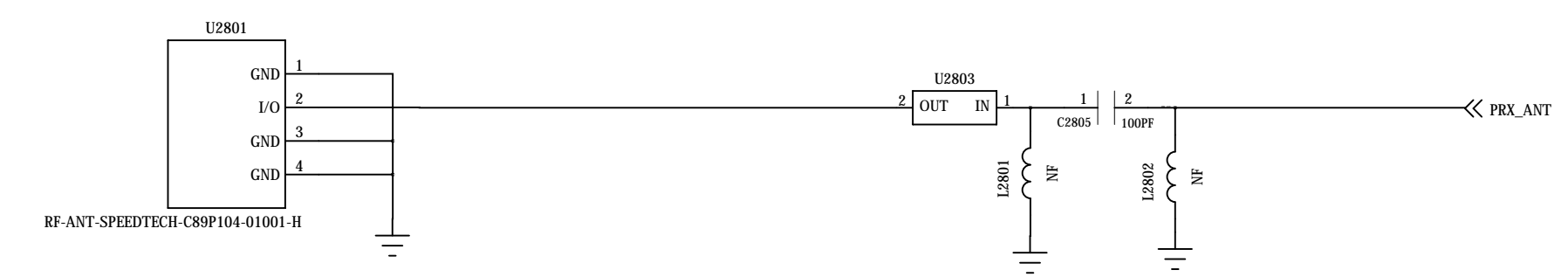
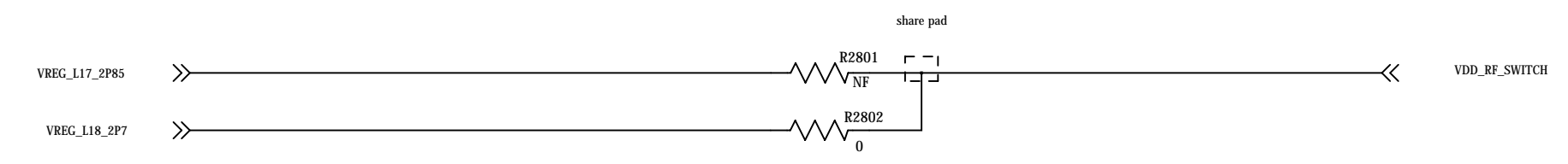


WTR4905 CONTROL, PWR & GND

If GSM is not supported, ground GP_DATA
 Note: FL2801 is a 5GHz LPF for Wi-Fi co-existence mitigation. Recommend a bypass option around FL2801 during evaluation until proven.

confirm attenuator
 6dB attenuator: R2703-R2702=150 OHM; R2701=36 OHM





	ANT_SWITCH_CTL0	ANT_SWITCH_CTL1
TRX_B7		
TRX_B40		
QFE2320_ANT		
TRX_B38_41		

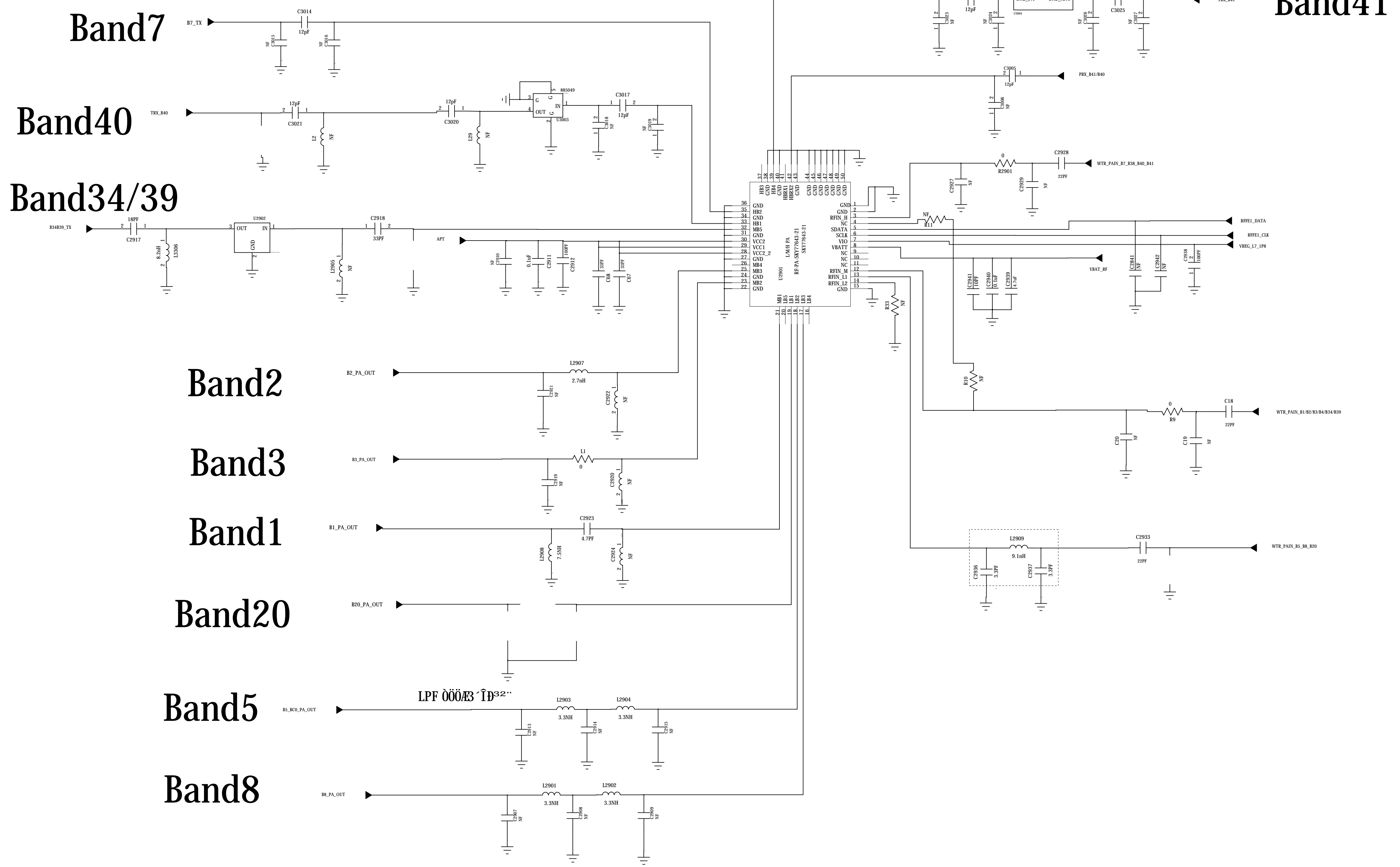
	ANT_SWITCH_CTL0	ANT_SWITCH_CTL1
TRX_B7		
TRX_B40		
QFE2320_ANT		
TRX_B38_41		

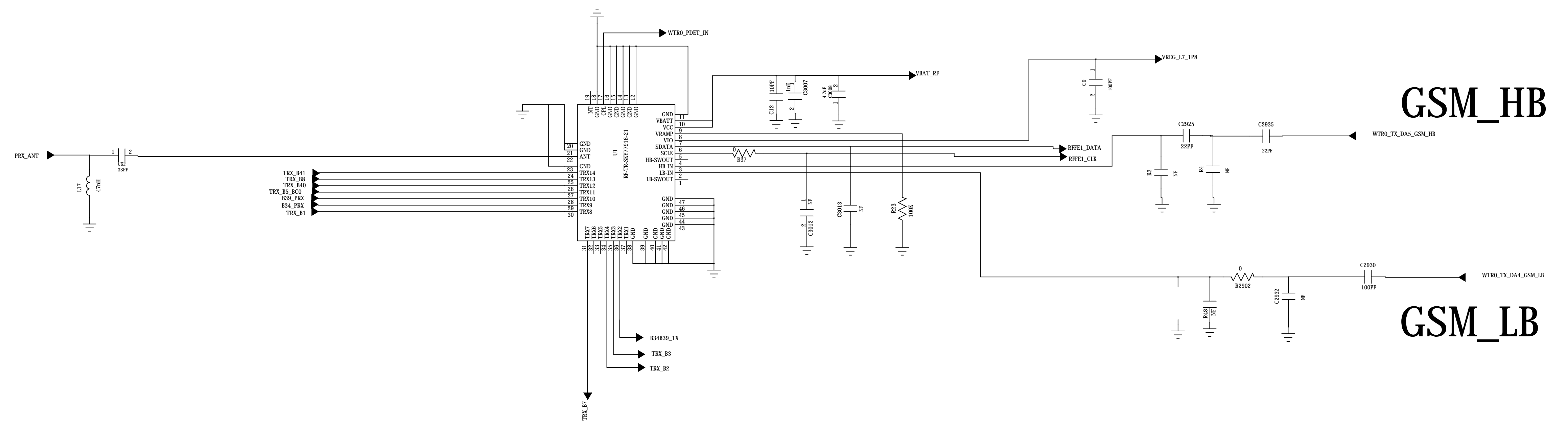
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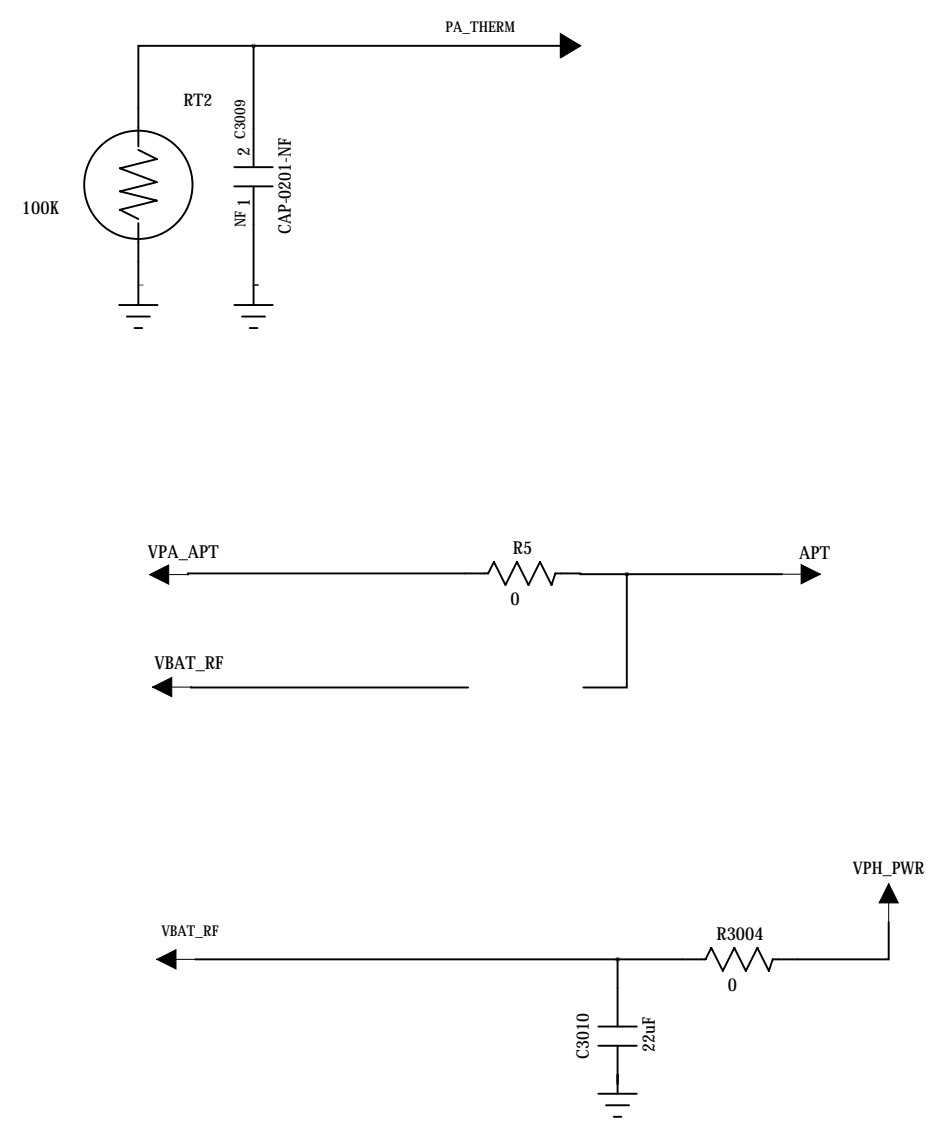
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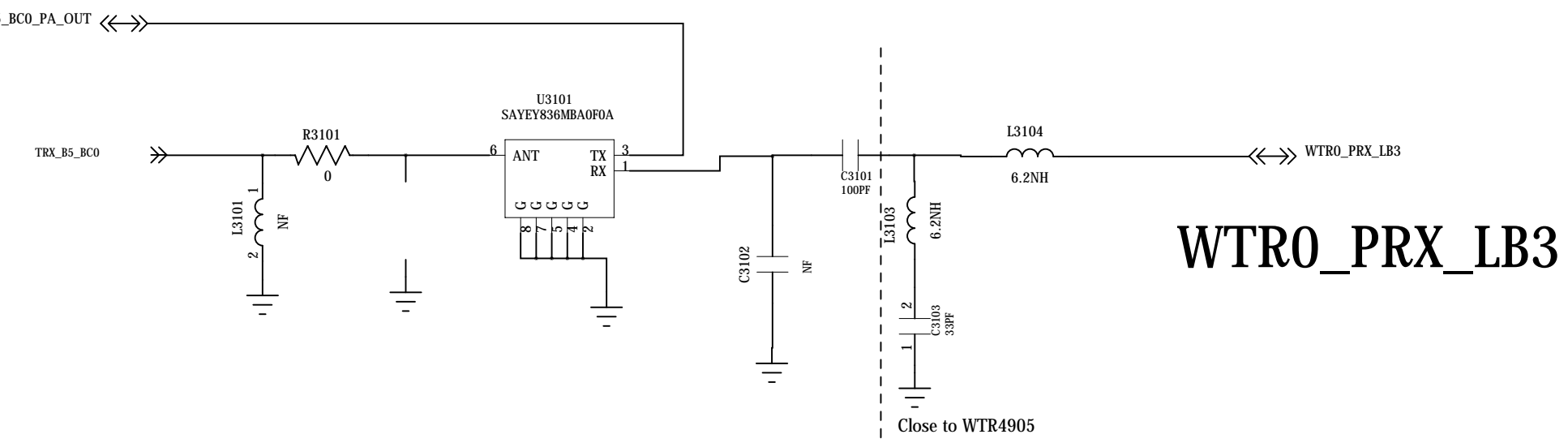


GSM_HB

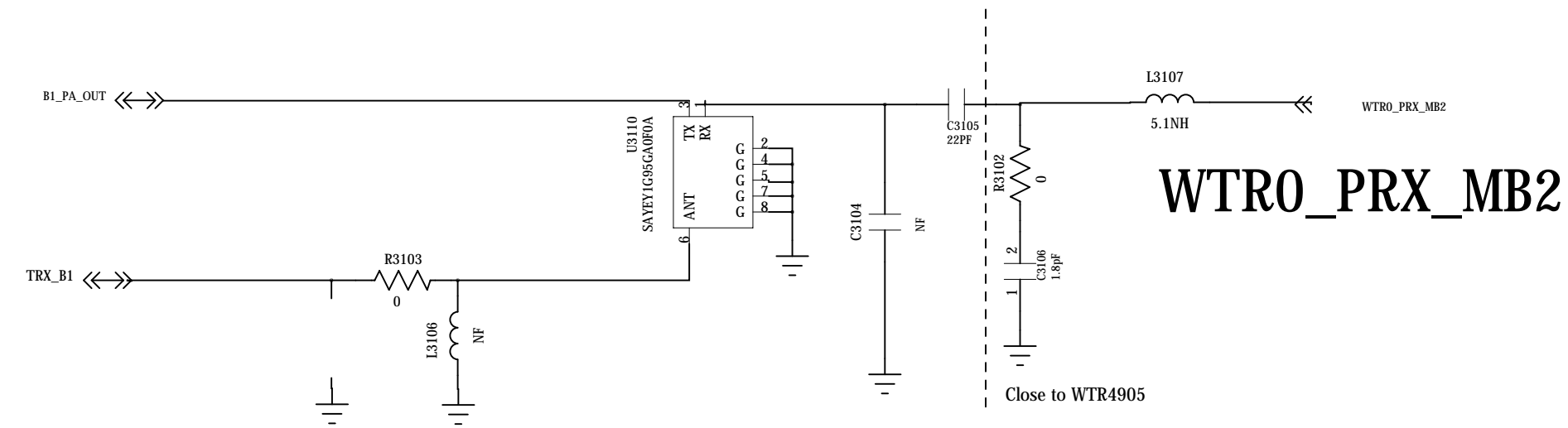
GSM_LB



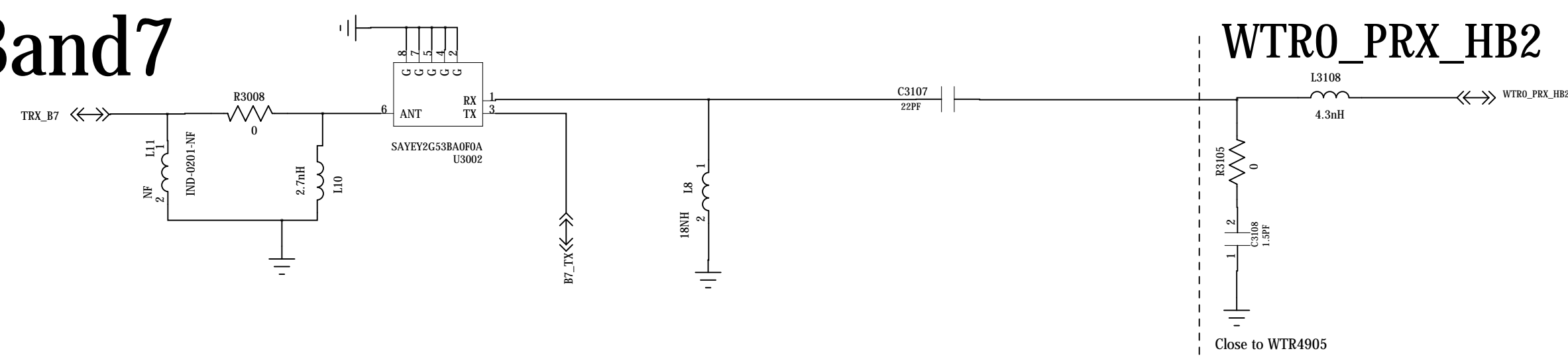
Band5



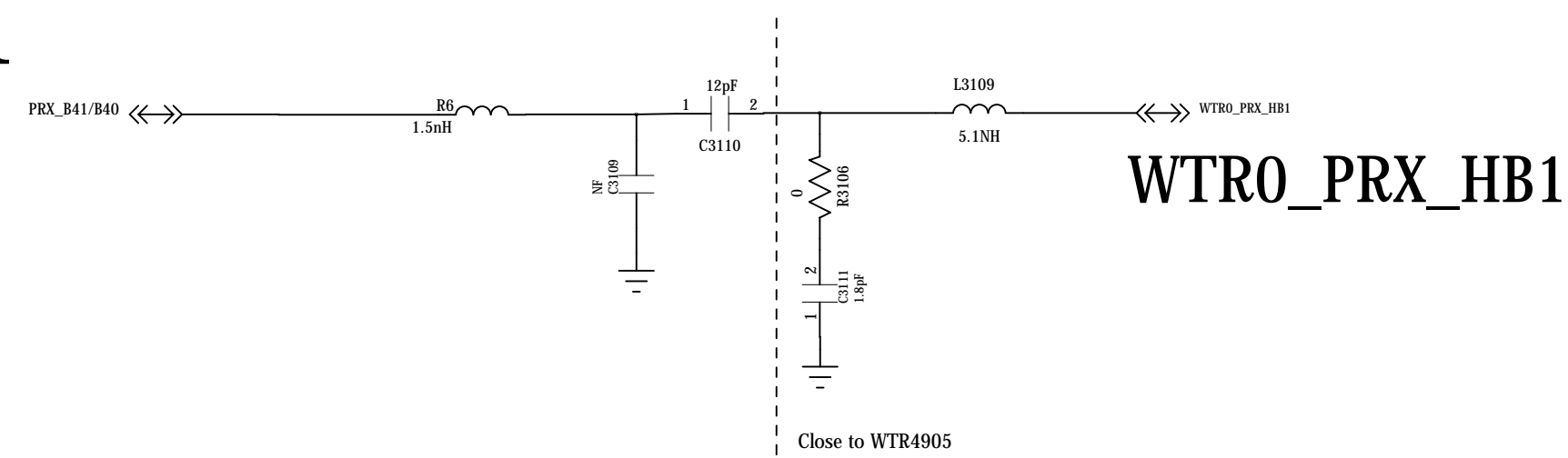
Band1



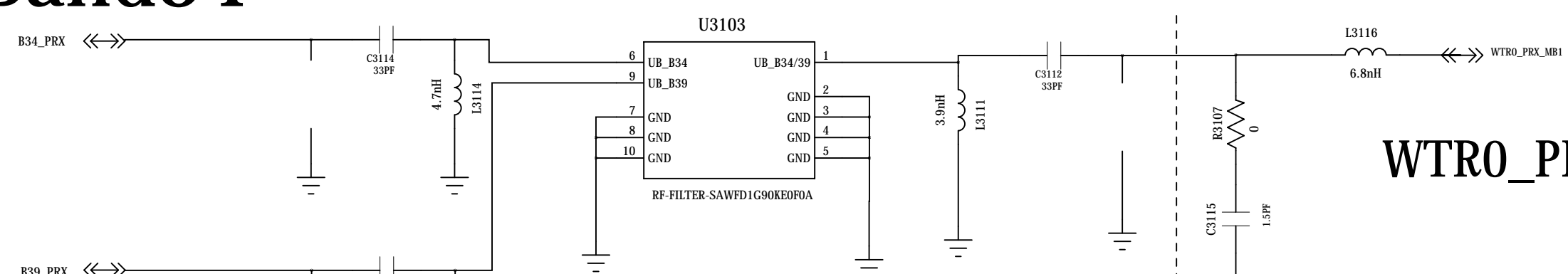
Band7



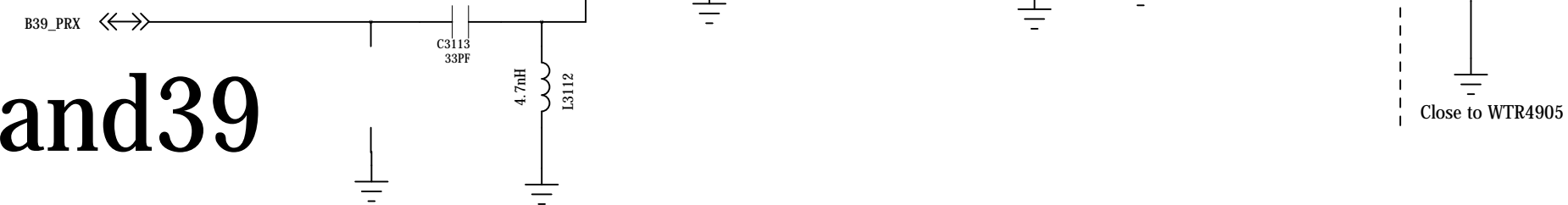
Band40/41



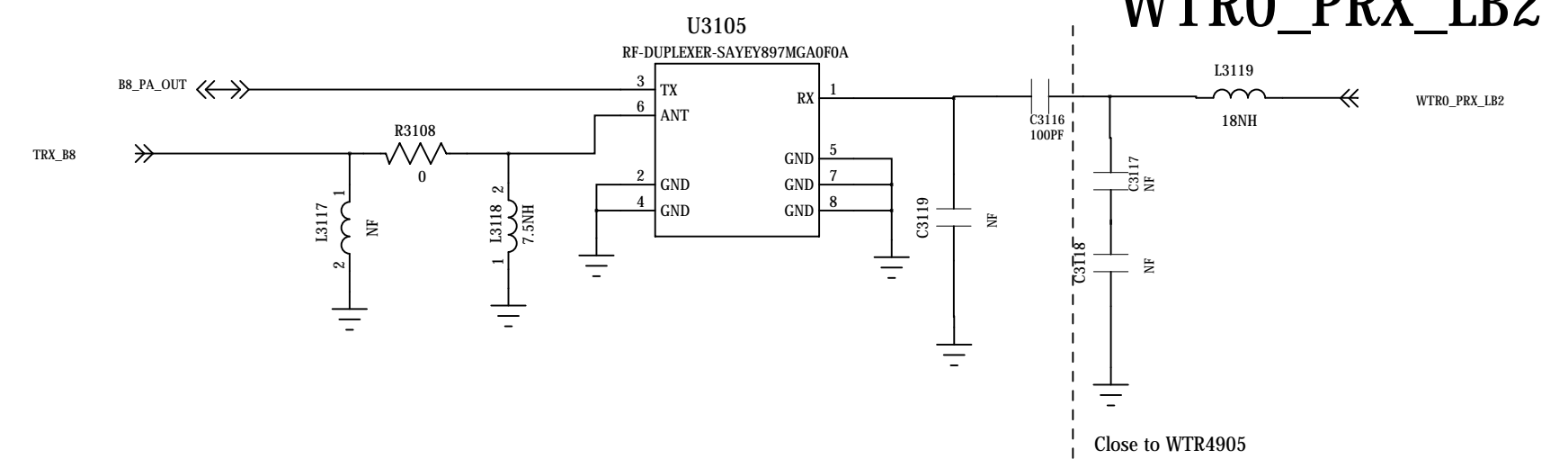
Band34



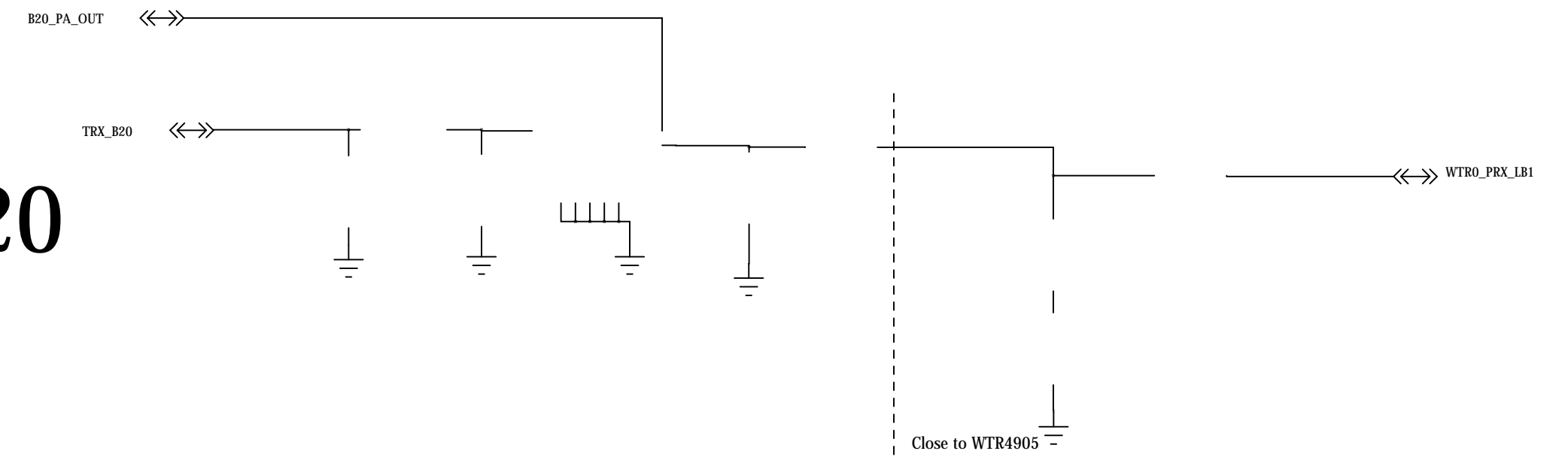
Band39



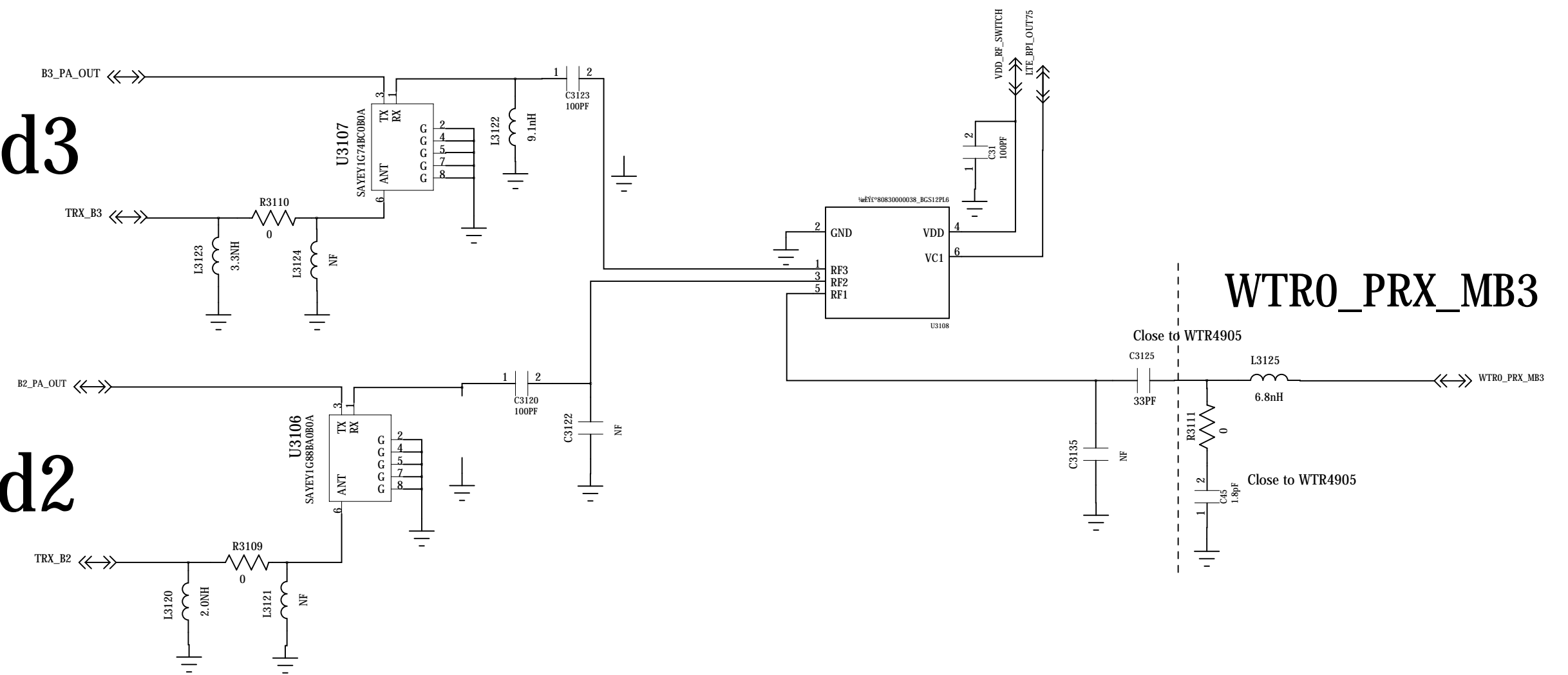
Band8



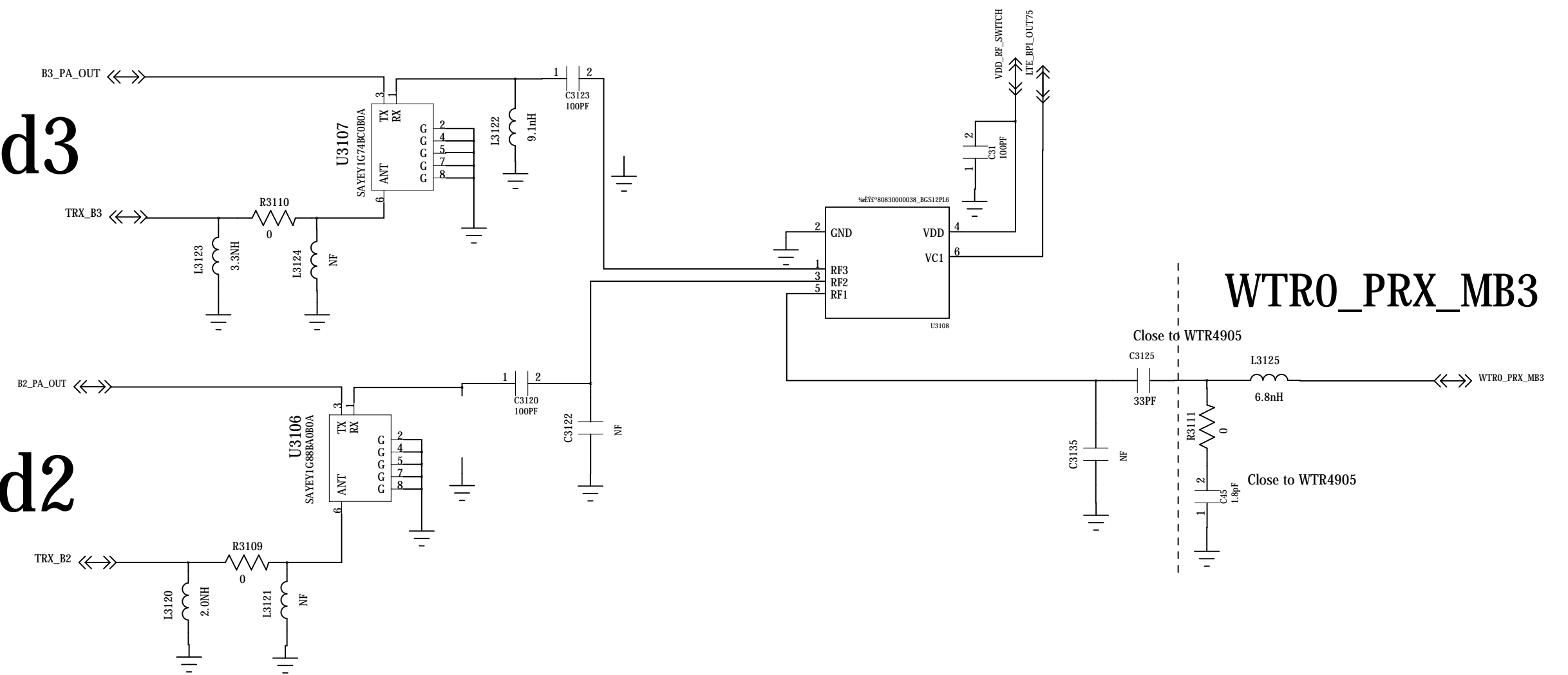
BandB20



Band3



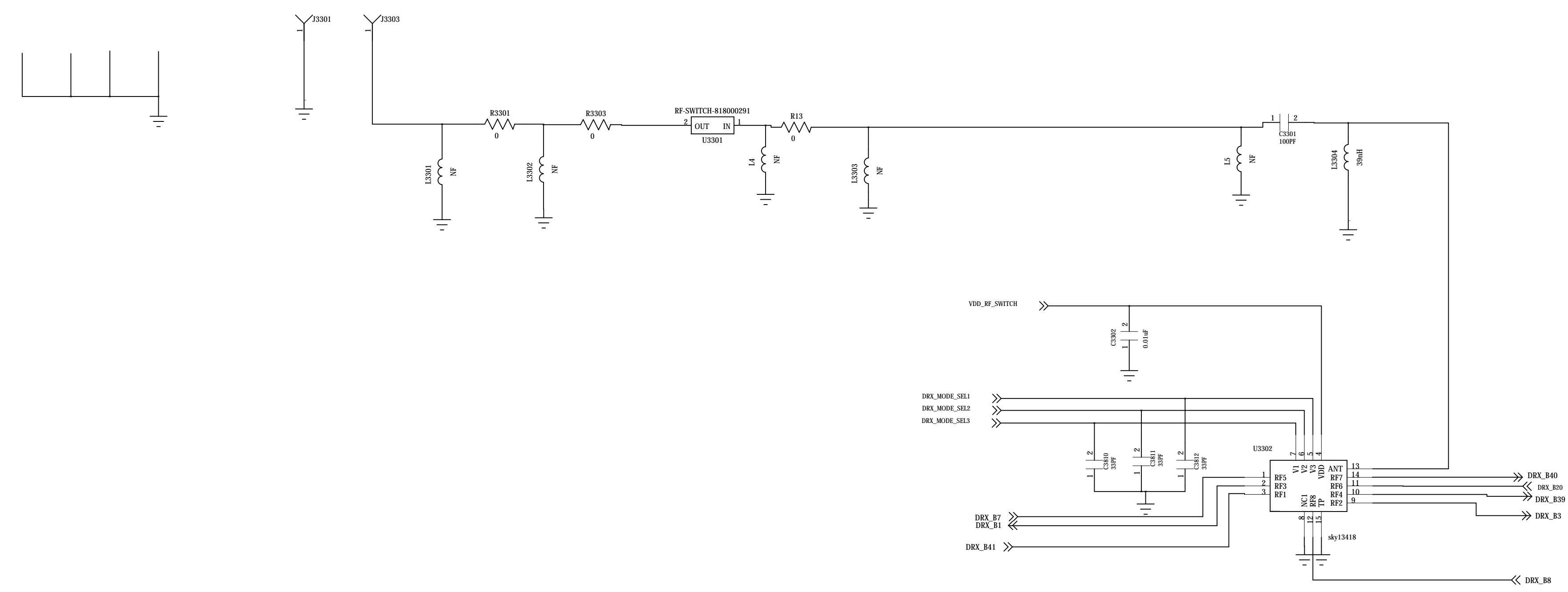
Band2



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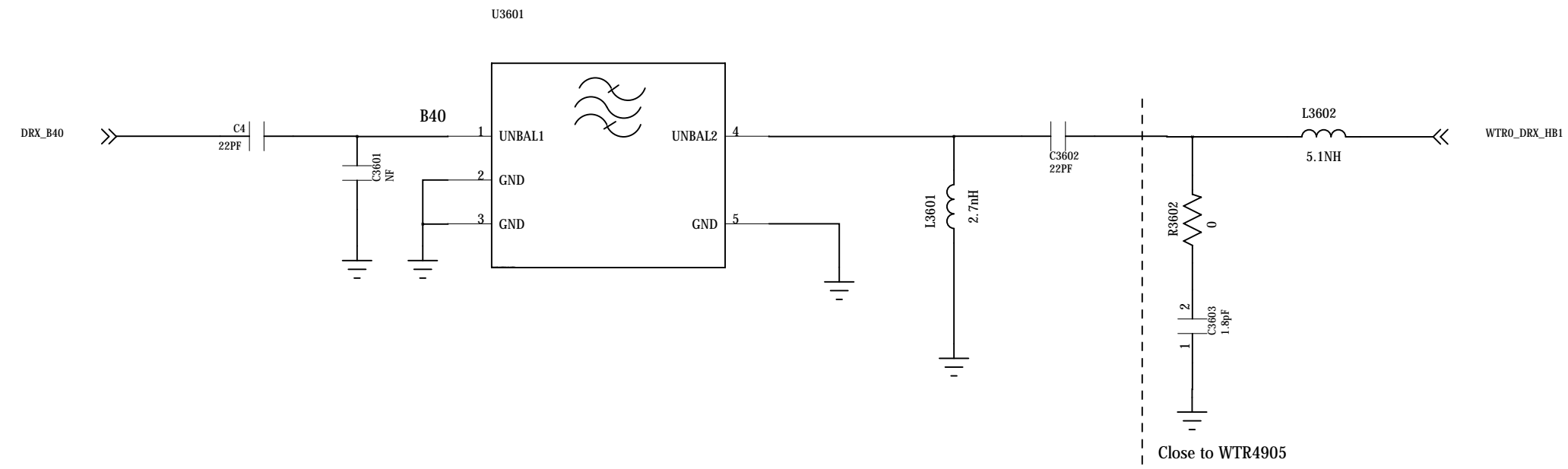
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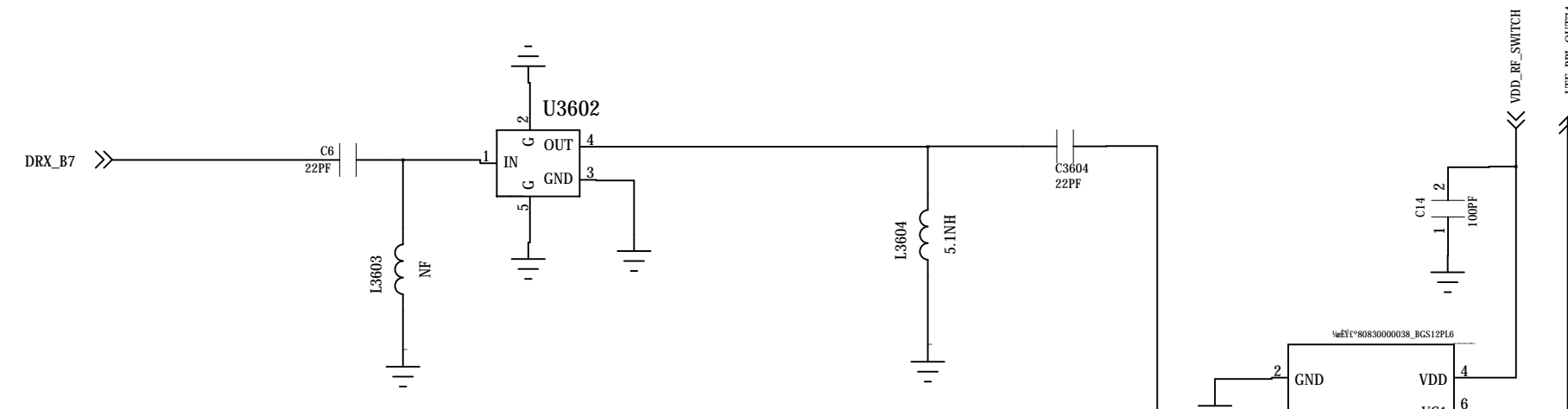
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Title		
Sheet	of	Rev
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Band40



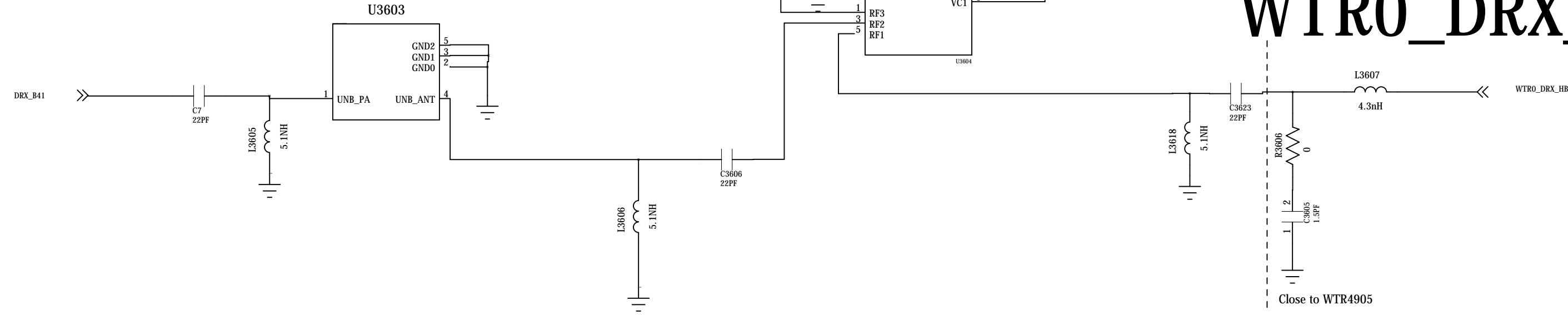
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Band7

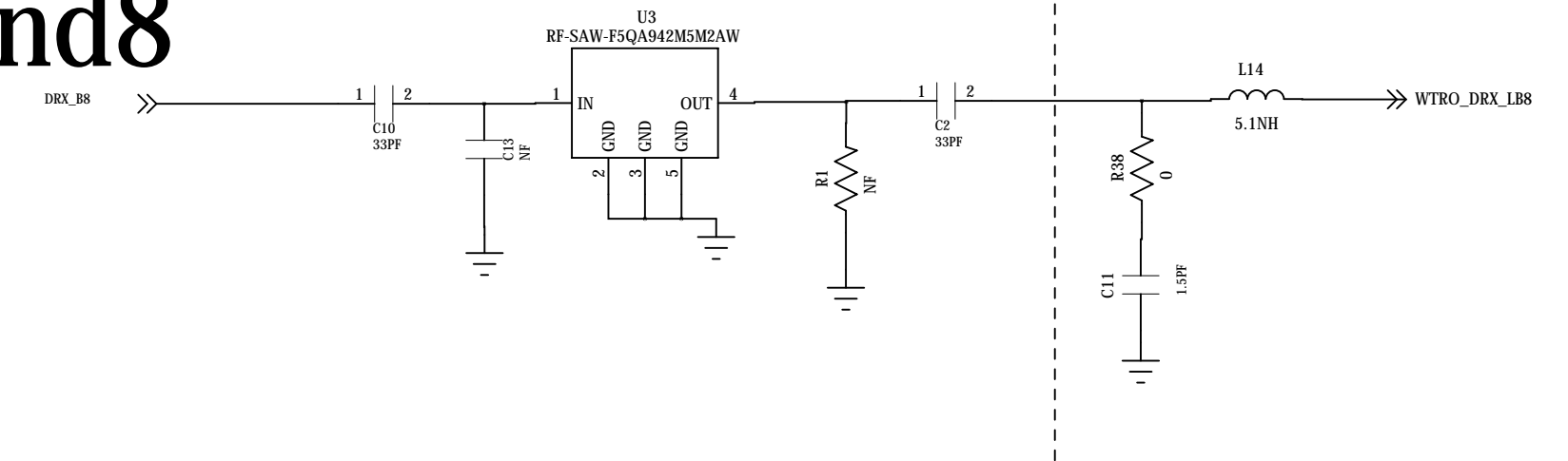


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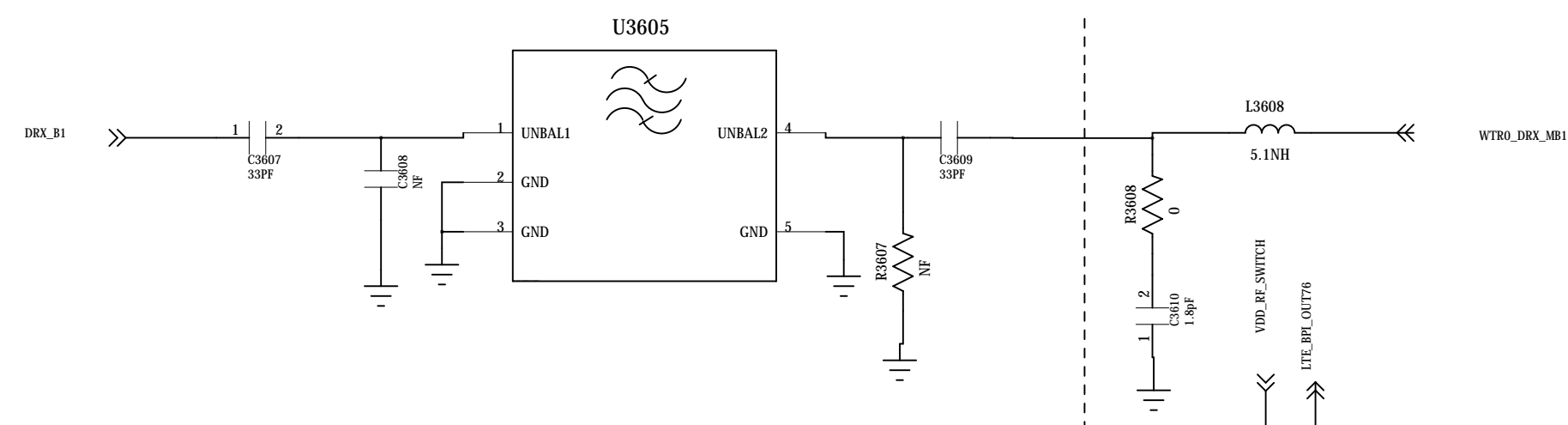
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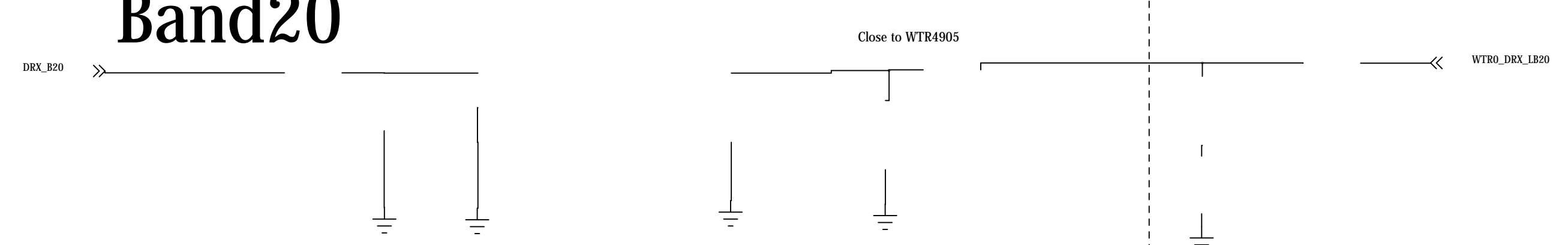


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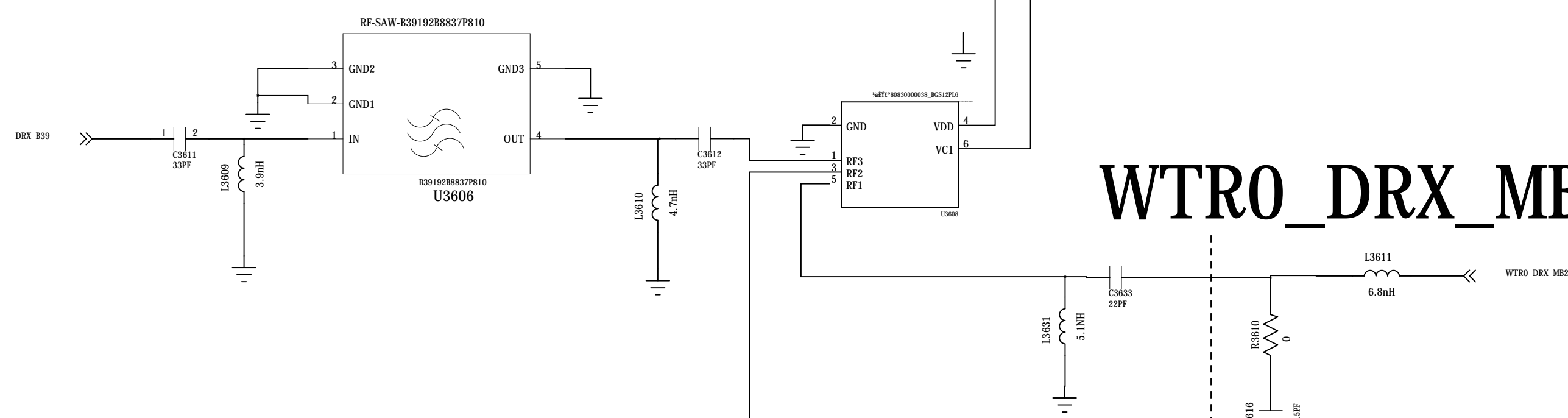


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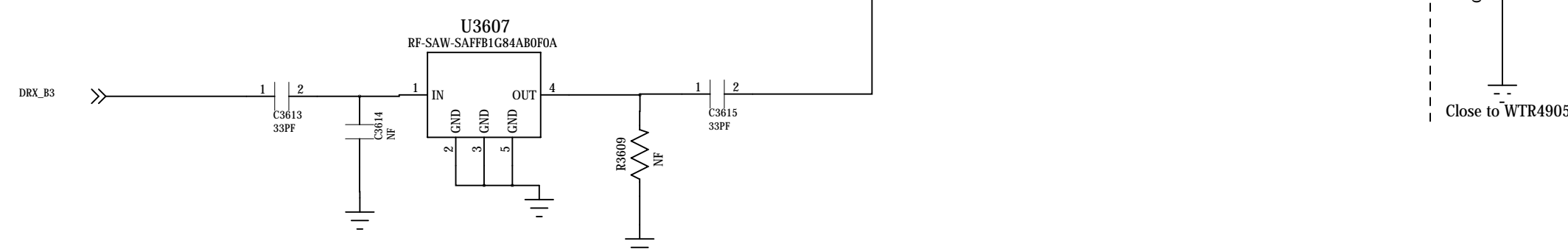


Band39



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Band3



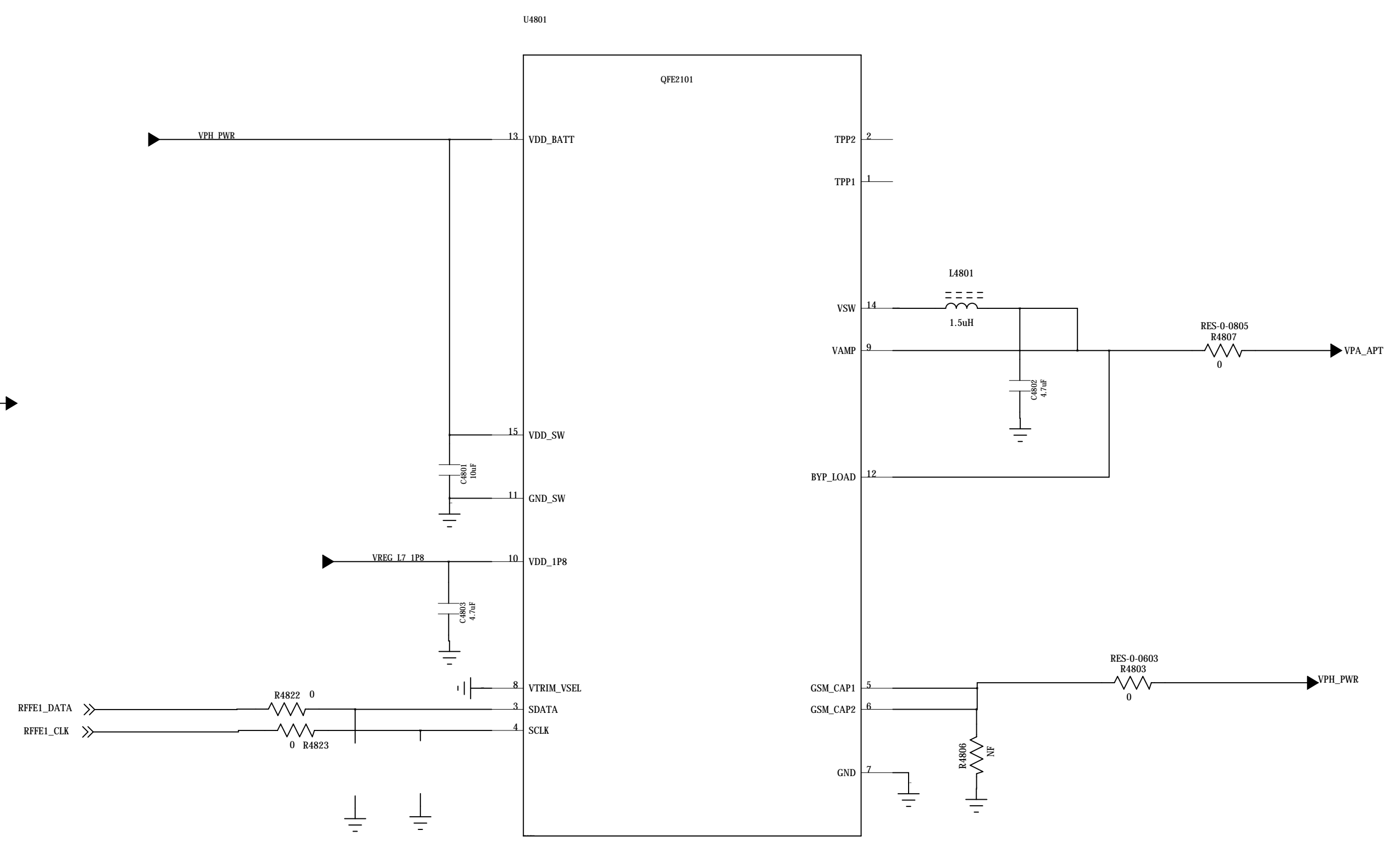
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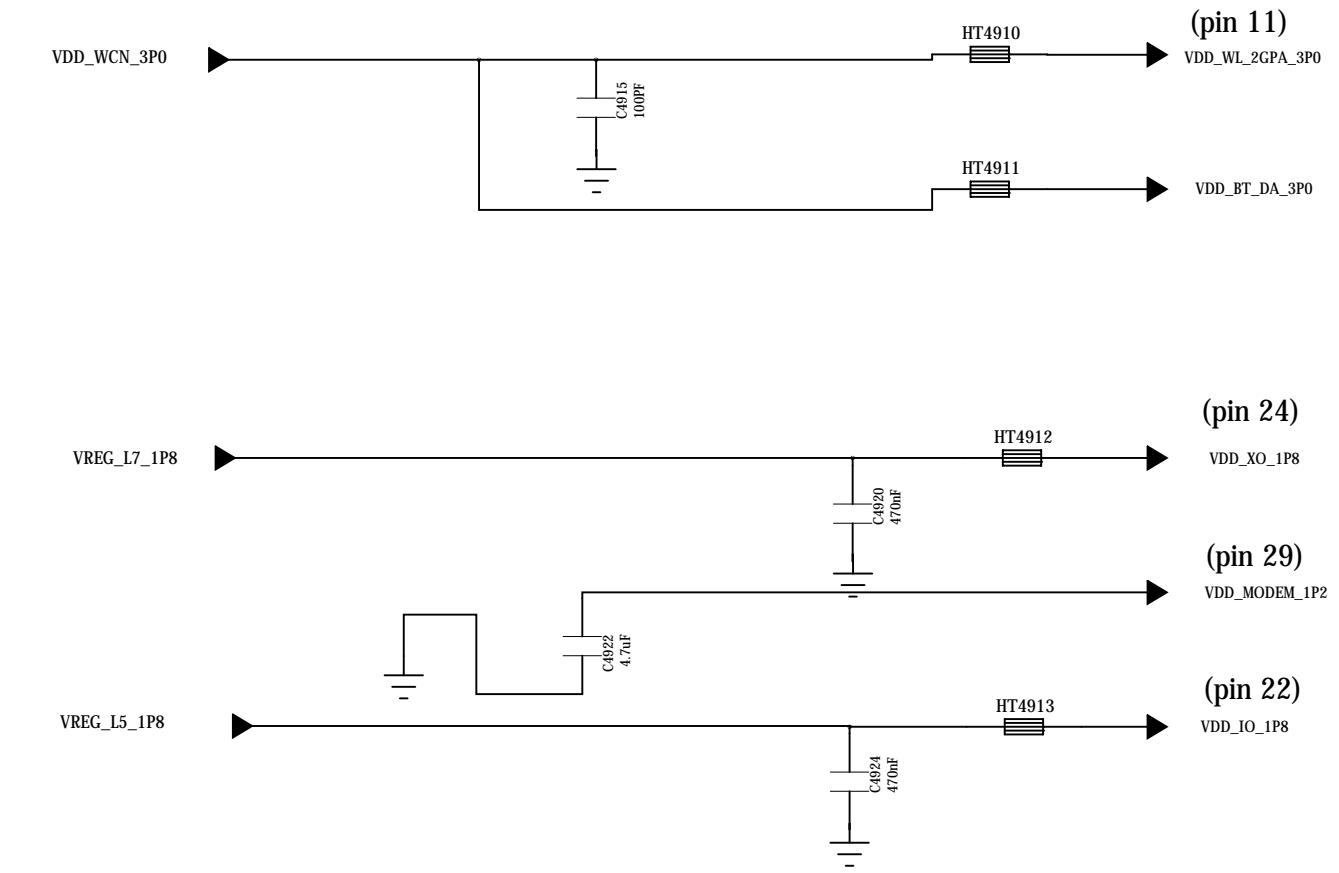
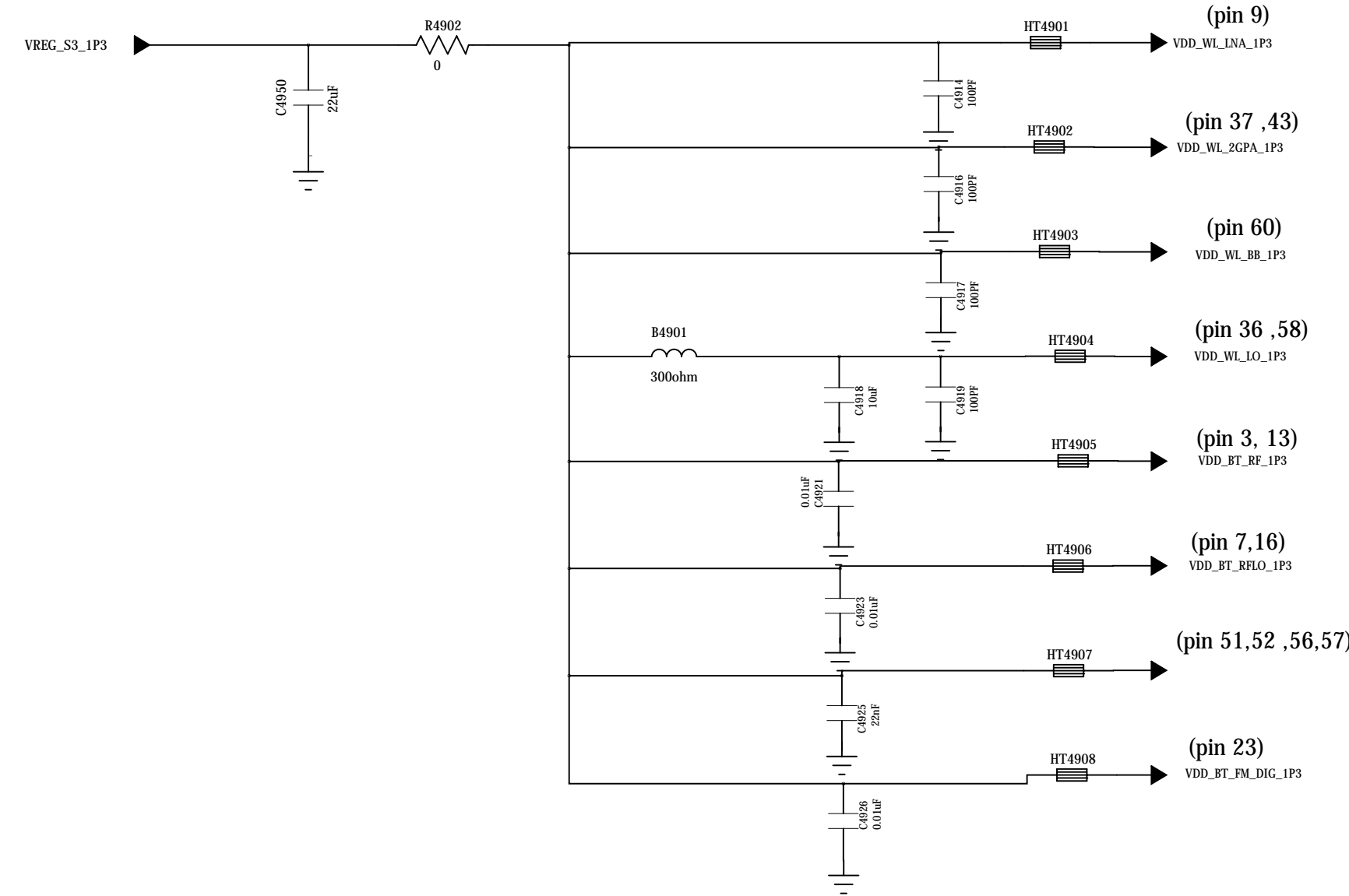
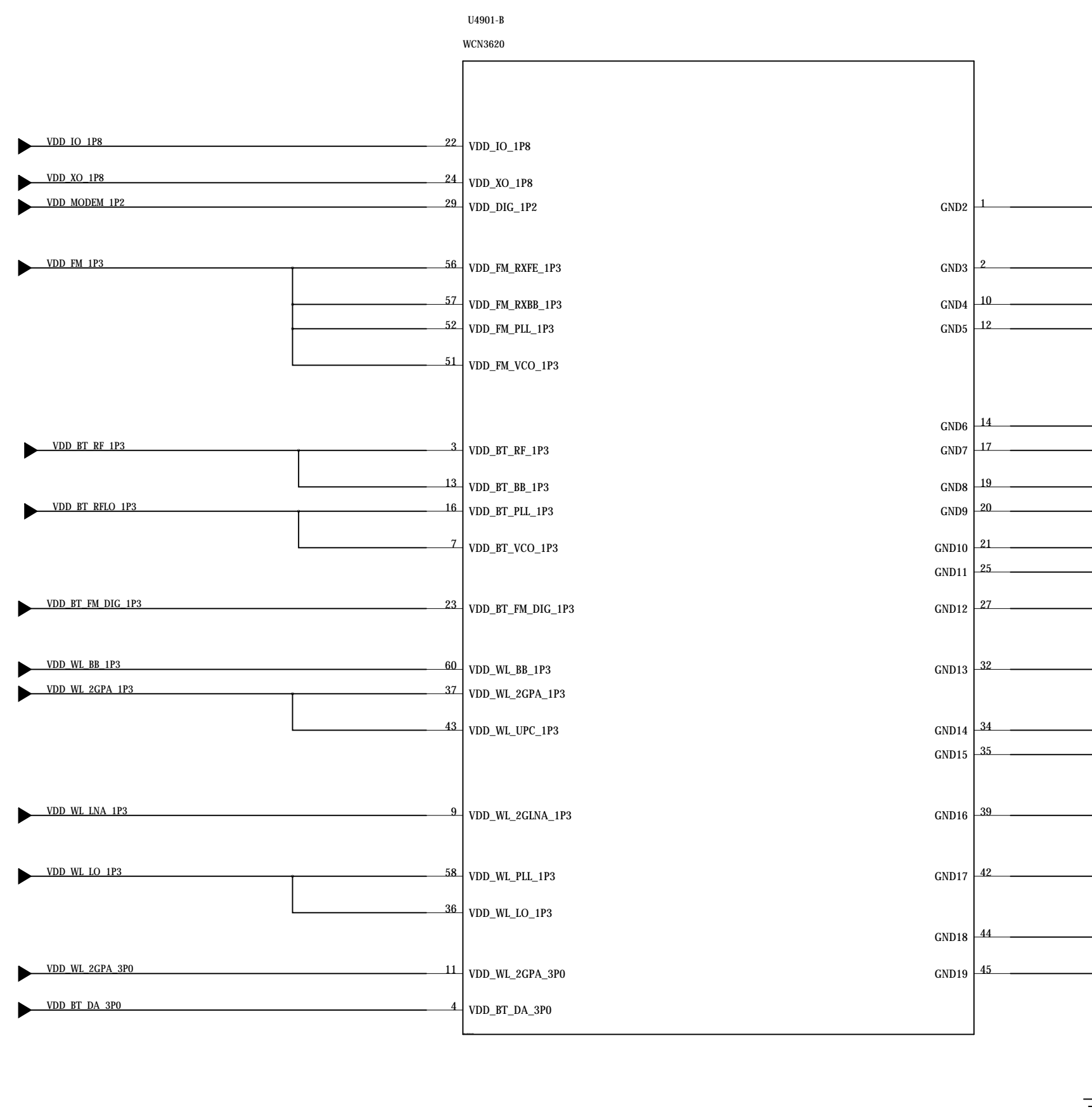
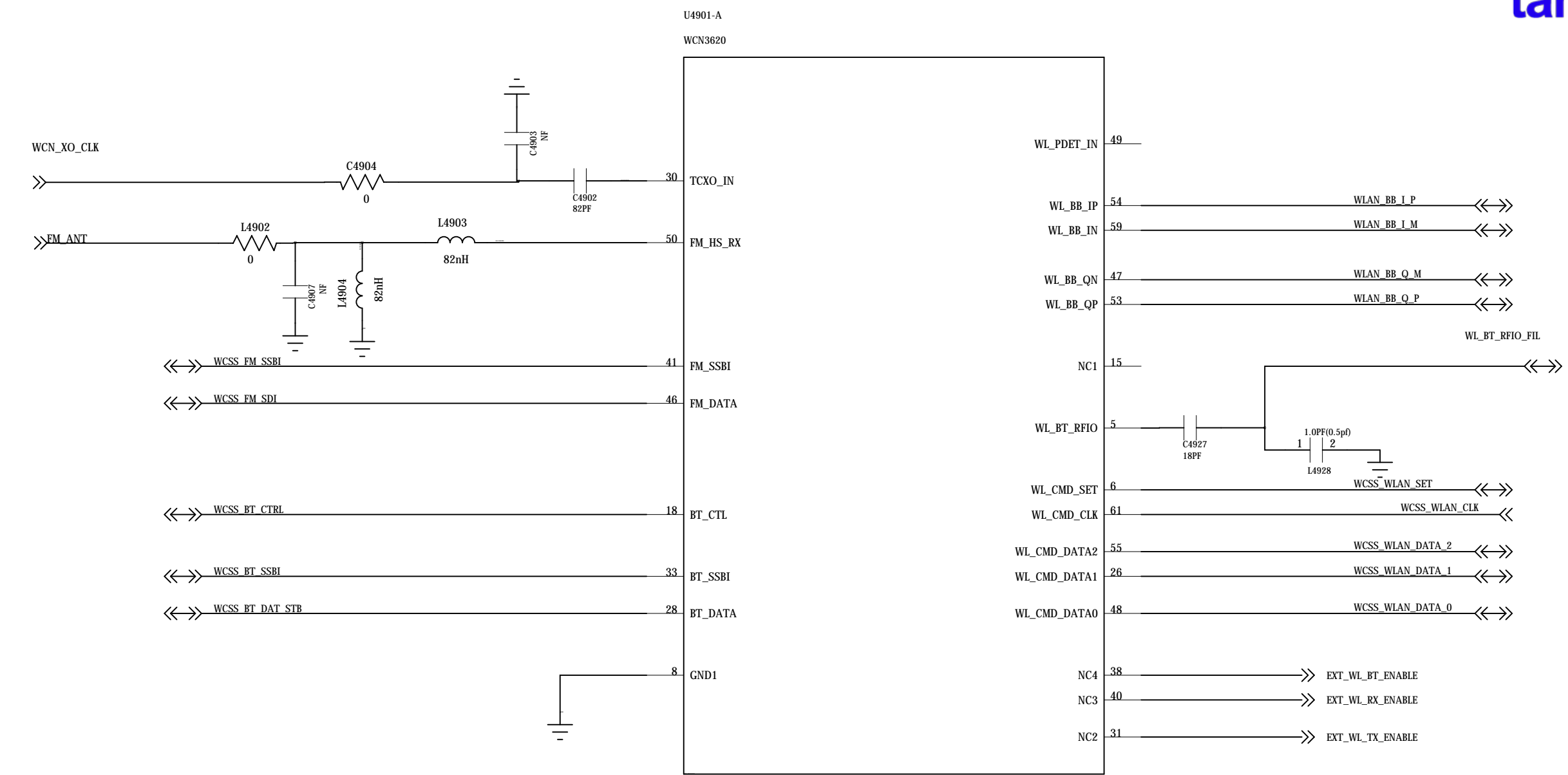
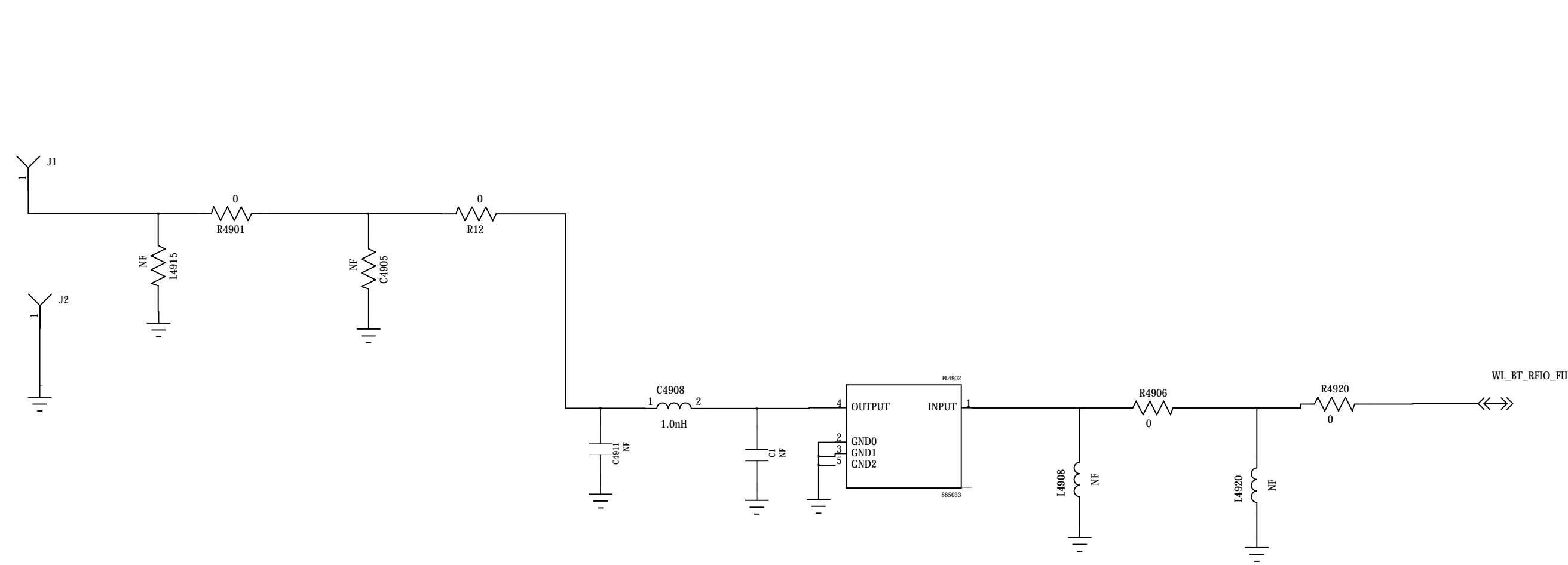
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Note: Use a single low impedance power plane/fill VPA for all ET PA VCC1/VCC2.
 Refer to 80-NA681-91 rev.B or later revisions for more layout details.



WIFI/BT

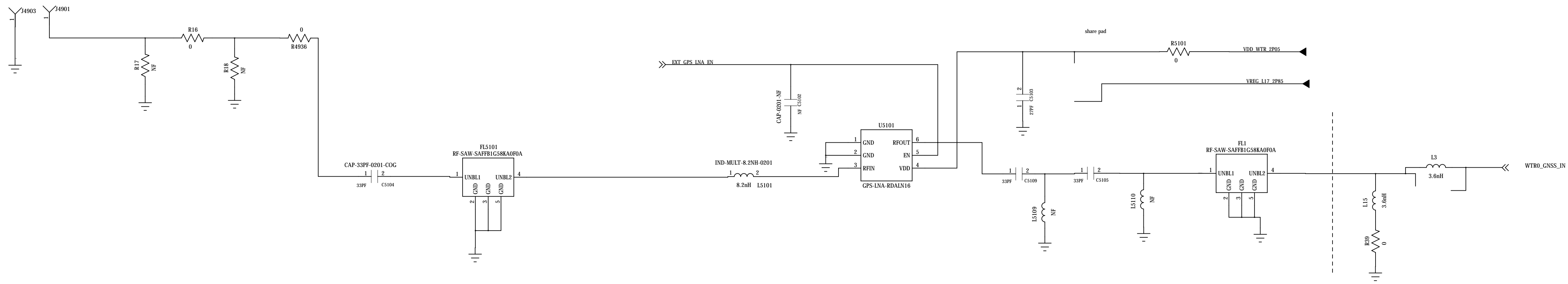


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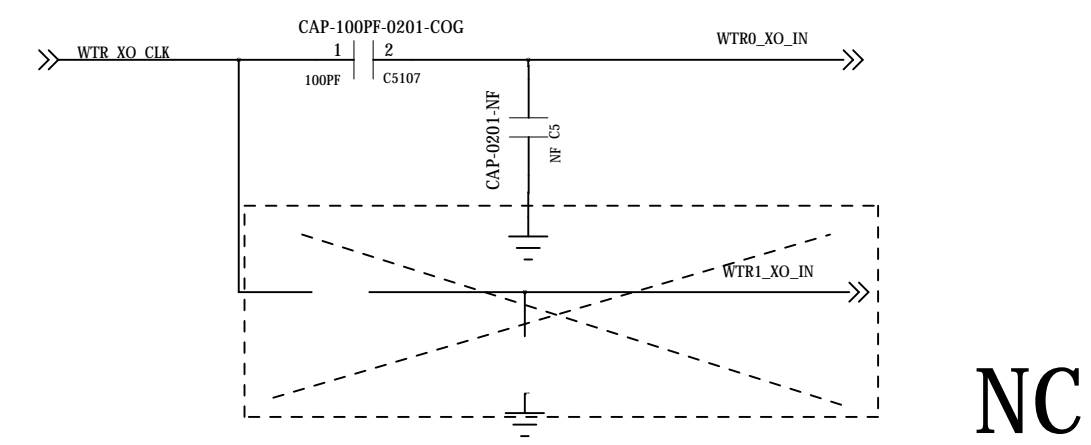
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GPS



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