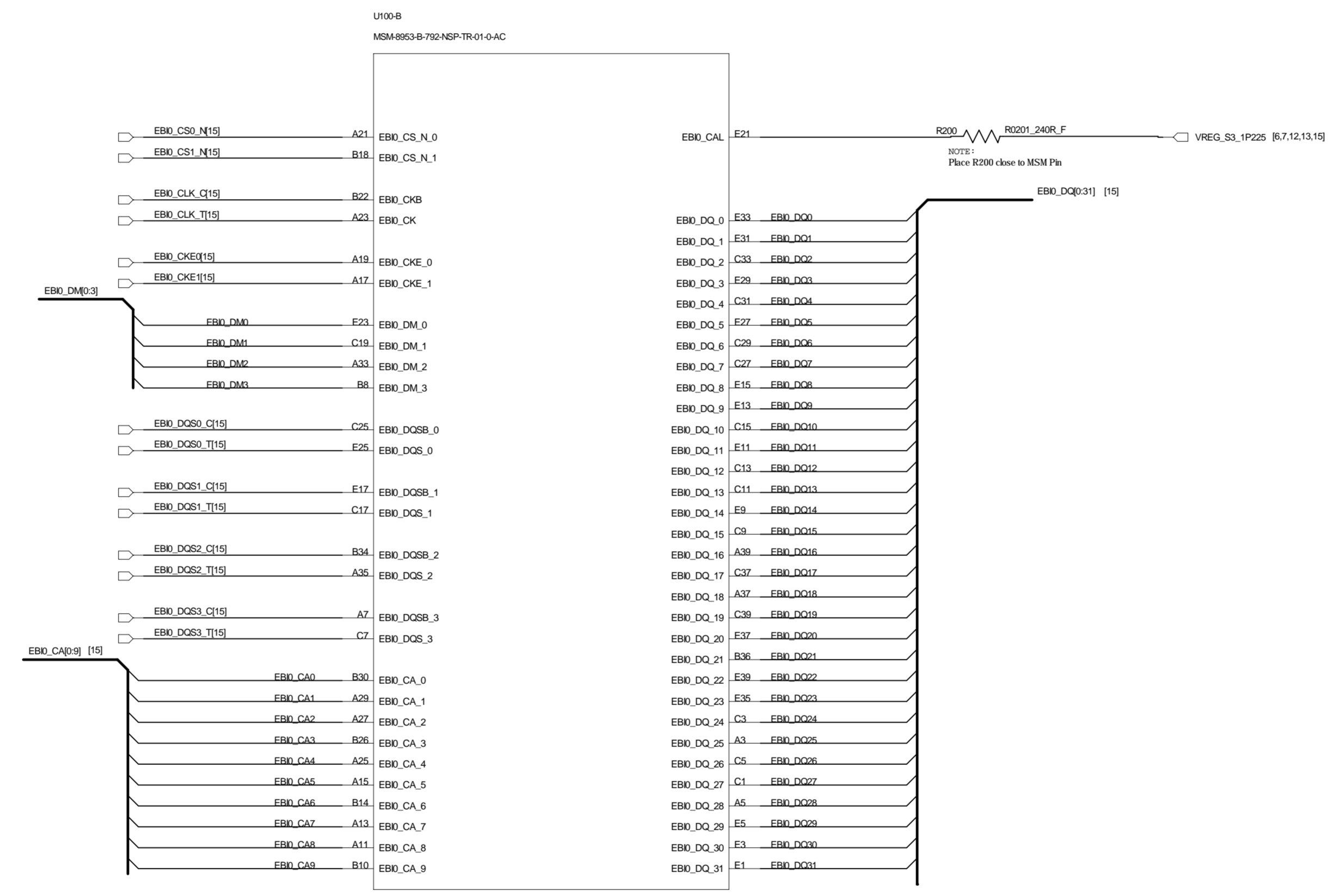


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MSM8953 Control

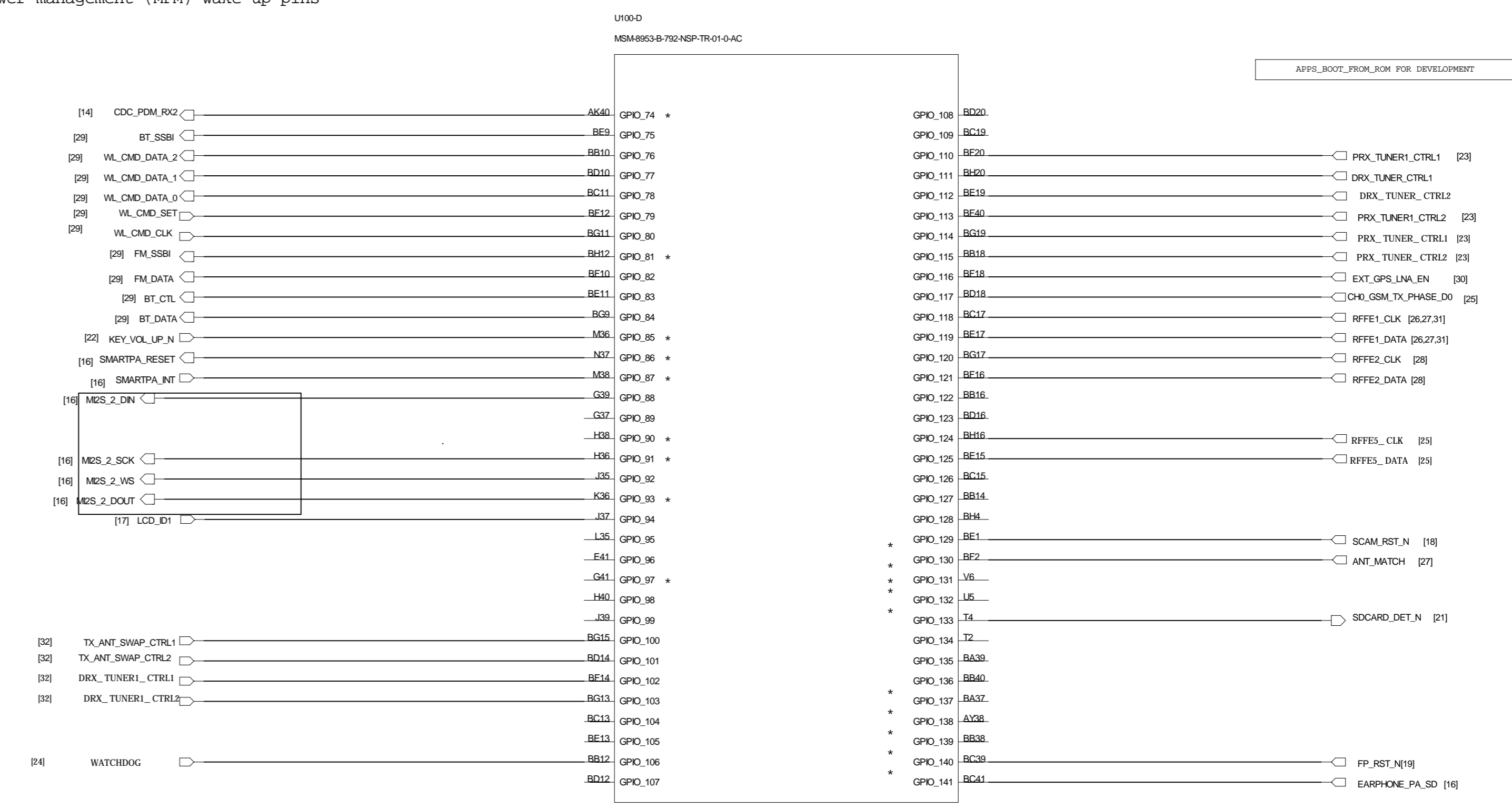
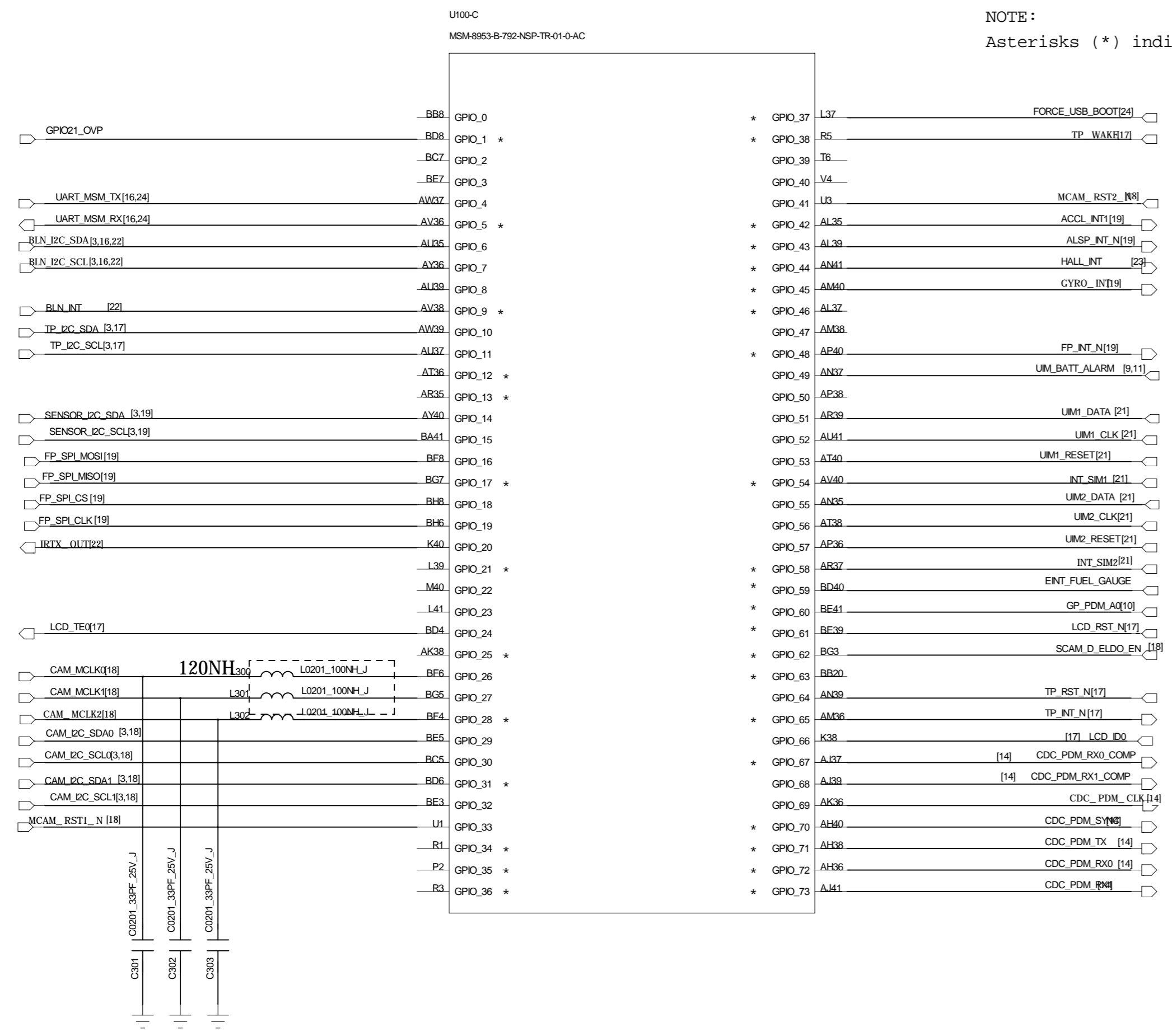


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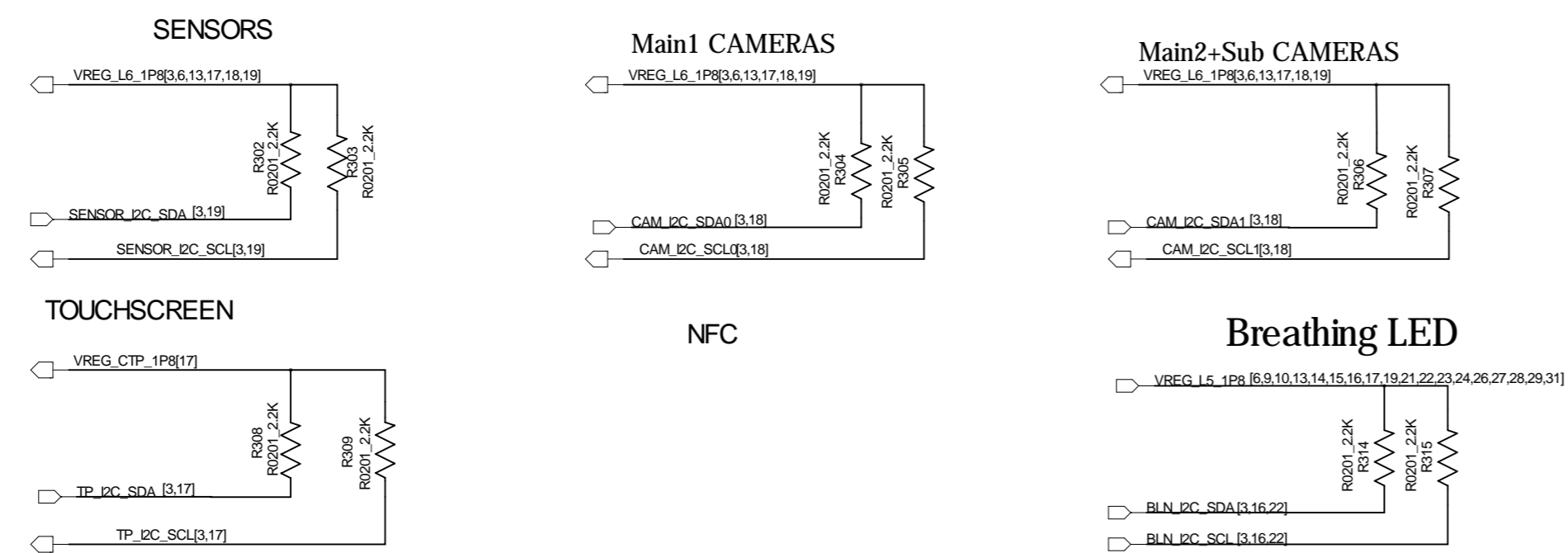
MSM8953 EBI

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I2C PULL-UP RESISTORS



NOTE:
Ensure SW sets these GPIOs (Sensor, CTP and Camera I2C bus) to inout pull down when the peripherals are powered off to eliminate leakage.

GPIO_37	FORCED_USB_BOOT
GPIO_106	MD00_DISABLE
GPIO_108	APPS_BOOT_FROM_ROM

BOOT_CONFIG[3:1]	BOOT_CONFIG
0b000	SDC1 -> SDC2 -> USB2.0
0b001	SDC2 -> SDC1 -> USB2.0
0b010	SDC1 -> USB2.0
0b011	USB2.0

Default Boot Config (0b000) is SDC1(eMMC)

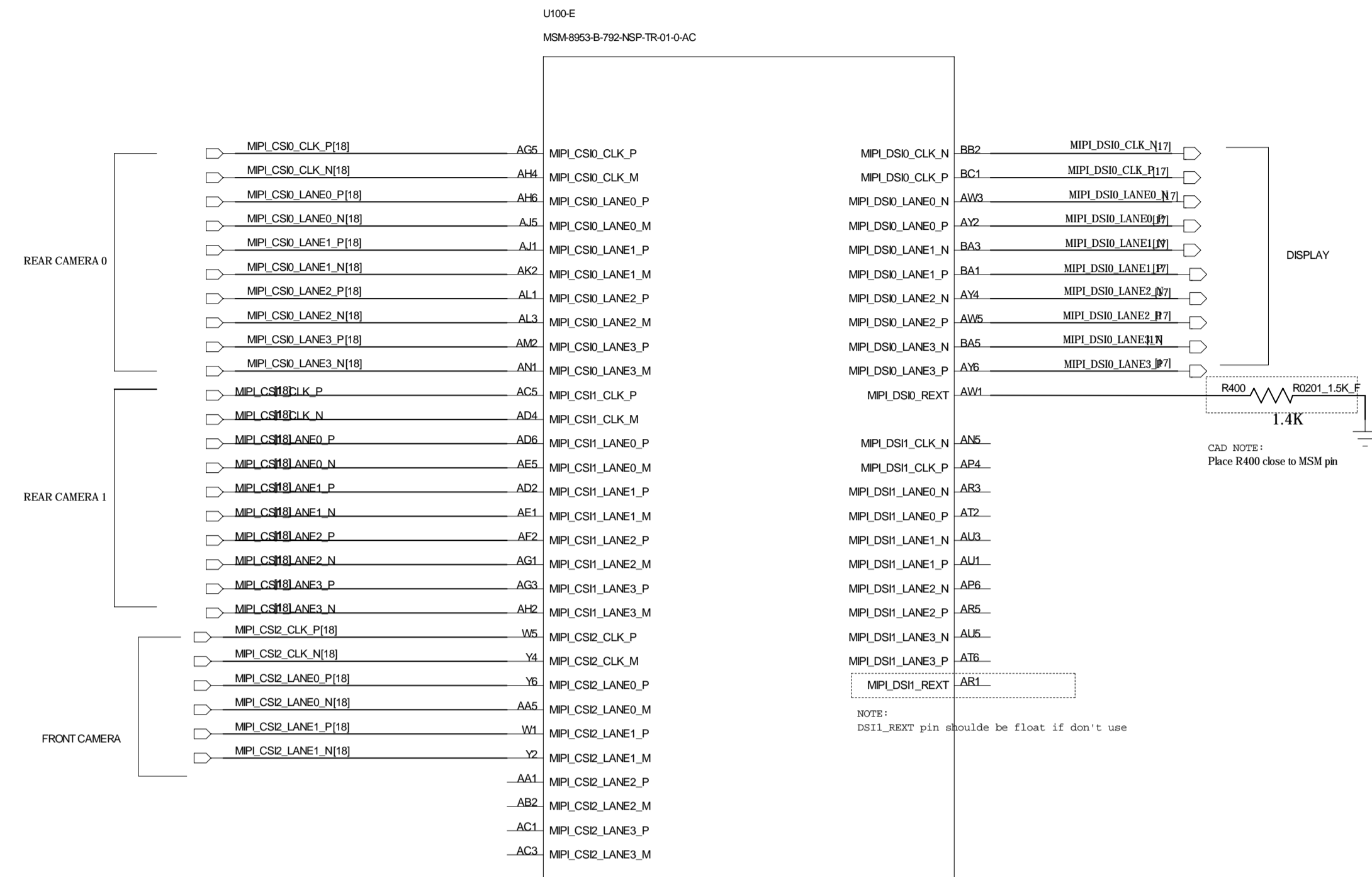
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MSM8953 GPIO



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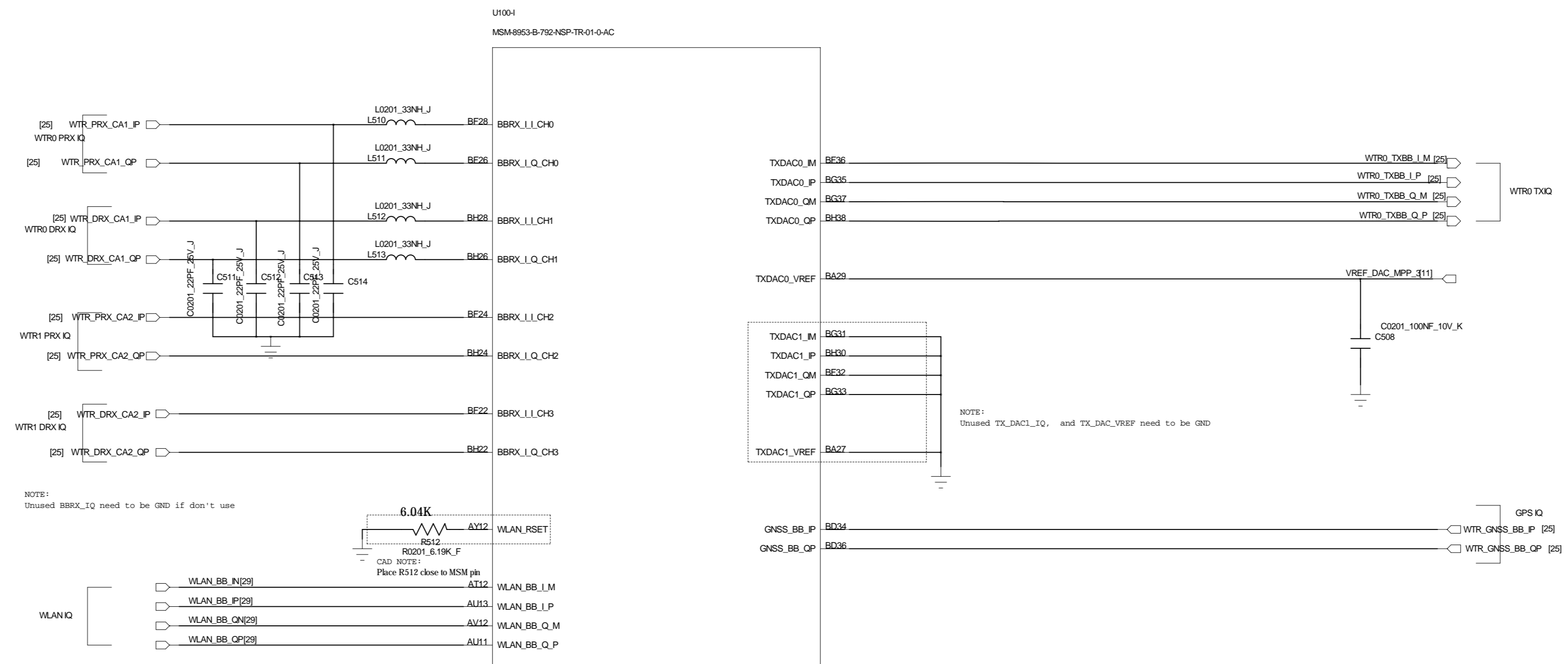
CSI Pin Name	CSI DPHY 4-lane	CSI DPHY 2+1 Mode	CSI CPHY 3Phase Mode
CSI0_3PHASE_PIN0	CSI0_CLKP	CSI0_2LANE_CLKP	NC
CSI0_3PHASE_PIN1	CSI0_CLKN	CSI0_2LANE_CLKN	CSI0_TRI0_A
CSI0_3PHASE_PIN2	CSI0_DP0	CSI0_2LANE_DP0	CSI0_TRI0_B
CSI0_3PHASE_PIN3	CSI0_DN0	CSI0_2LANE_DN0	CSI0_TRI0_C
CSI0_3PHASE_PIN4	CSI0_DP1	CSI0_2LANE_DP1	CSI0_TRI1_A
CSI0_3PHASE_PIN5	CSI0_DN1	CSI0_2LANE_DN1	CSI0_TRI1_B
CSI0_3PHASE_PIN6	CSI0_DP2	CSI0_1LANE_DP0	CSI0_TRI1_C
CSI0_3PHASE_PIN7	CSI0_DN2	CSI0_1LANE_DN0	CSI0_TRI2_A
CSI0_3PHASE_PIN8	CSI0_DP3	CSI0_1LANE_CLKP	CSI0_TRI2_B
CSI0_3PHASE_PIN9	CSI0_CLKN	CSI0_2LANE_CLKN	CSI0_TRI2_C
CSI1_3PHASE_PIN1	CSI1_CLKN	CSI1_2LANE_CLKN	CSI1_TRI0_A
CSI1_3PHASE_PIN2	CSI1_DP0	CSI1_2LANE_DP0	CSI1_TRI0_B
CSI1_3PHASE_PIN3	CSI1_DN0	CSI1_2LANE_DN0	CSI1_TRI0_C
CSI1_3PHASE_PIN4	CSI1_DP1	CSI1_2LANE_DP1	CSI1_TRI1_A
CSI1_3PHASE_PIN5	CSI1_DN1	CSI1_2LANE_DN1	CSI1_TRI1_B
CSI1_3PHASE_PIN6	CSI1_DP2	CSI1_1LANE_DP0	CSI1_TRI1_C
CSI1_3PHASE_PIN7	CSI1_DN2	CSI1_1LANE_DN0	CSI1_TRI2_A
CSI1_3PHASE_PIN8	CSI1_DP3	CSI1_1LANE_CLKP	CSI1_TRI2_B
CSI1_3PHASE_PIN9	CSI1_CLKN	CSI1_2LANE_CLKN	CSI1_TRI2_C
CSI2_3PHASE_PIN1	CSI2_CLKN	CSI2_2LANE_CLKN	CSI2_TRI0_A
CSI2_3PHASE_PIN2	CSI2_DP0	CSI2_2LANE_DP0	CSI2_TRI0_B
CSI2_3PHASE_PIN3	CSI2_DN0	CSI2_2LANE_DN0	CSI2_TRI0_C
CSI2_3PHASE_PIN4	CSI2_DP1	CSI2_2LANE_DP1	CSI2_TRI1_A
CSI2_3PHASE_PIN5	CSI2_DN1	CSI2_2LANE_DN1	CSI2_TRI1_B
CSI2_3PHASE_PIN6	CSI2_DP2	CSI2_1LANE_DP0	CSI2_TRI1_C
CSI2_3PHASE_PIN7	CSI2_DN2	CSI2_1LANE_DN0	CSI2_TRI2_A
CSI2_3PHASE_PIN8	CSI2_DP3	CSI2_1LANE_CLKP	CSI2_TRI2_B
CSI2_3PHASE_PIN9	CSI2_DN3	CSI2_1LANE_CLKN	CSI2_TRI2_C

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MSM8953 MIPI

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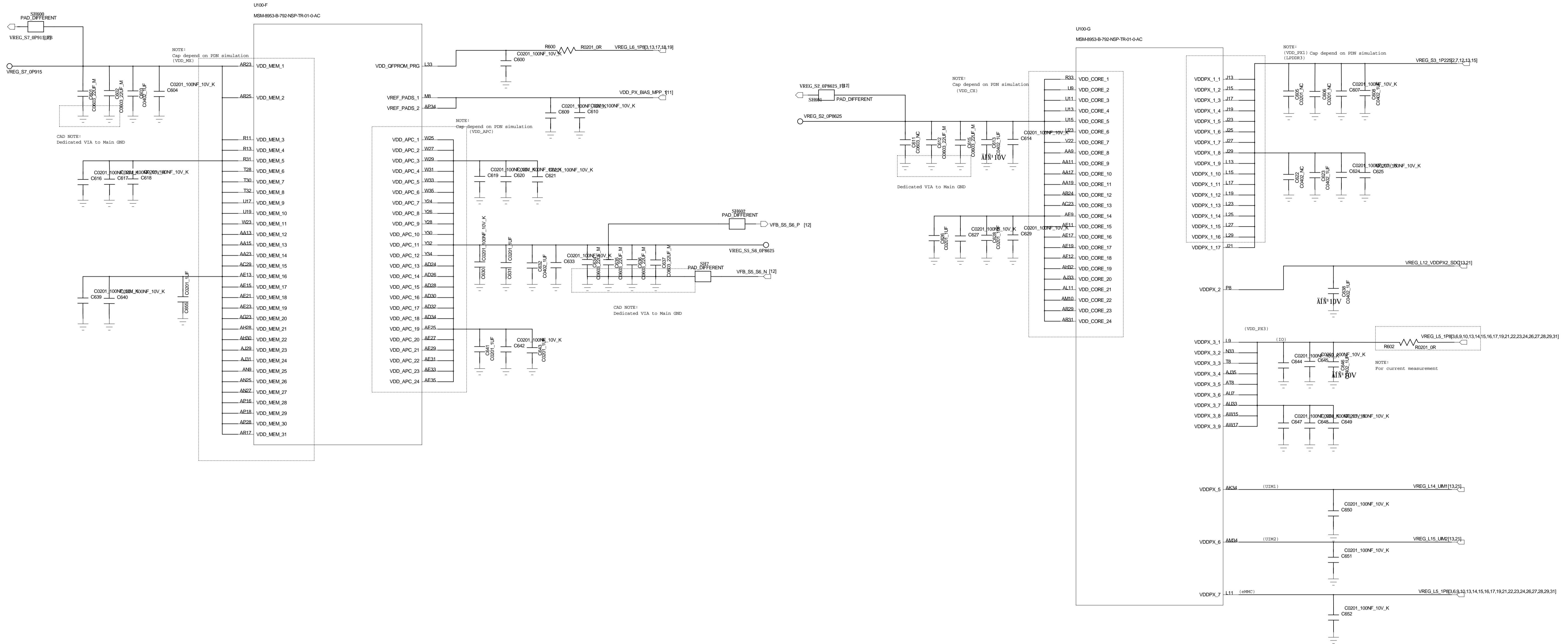


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MSM8953 RF

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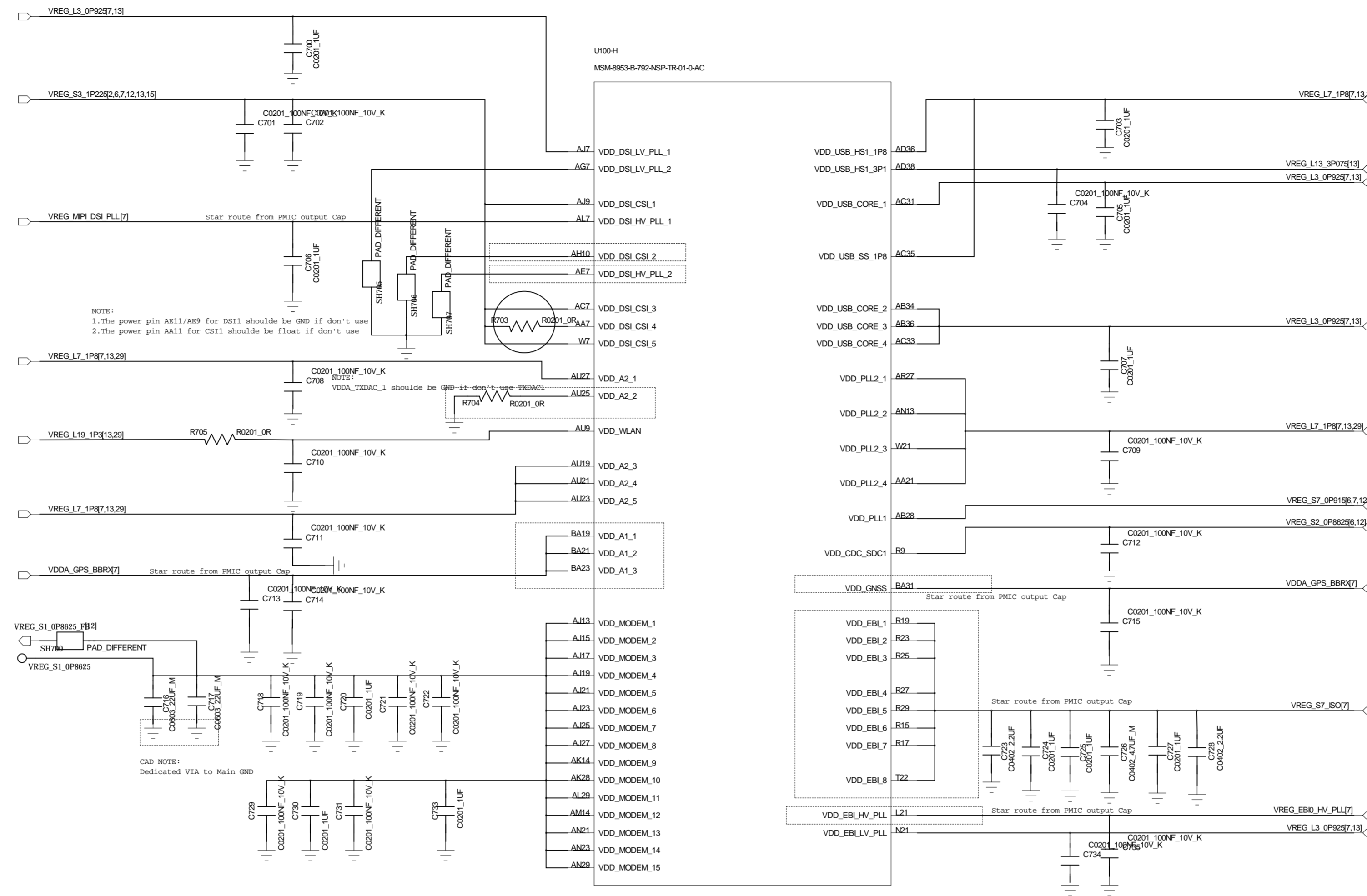
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MSM8953 POWER1

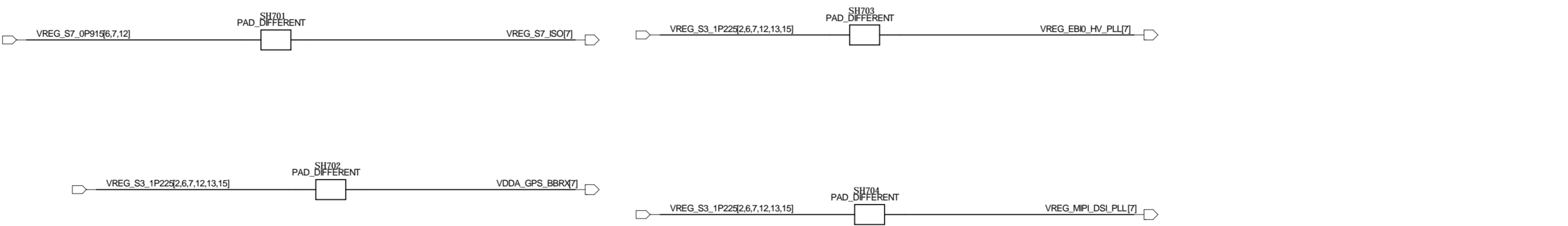
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NOTES:
 1. The power pin A11/A189 for DSI1 should be GND if don't use
 2. The power pin A11 for CSI1 should be float if don't use

CAD NOTE:
 Dedicated VIA to Main GND



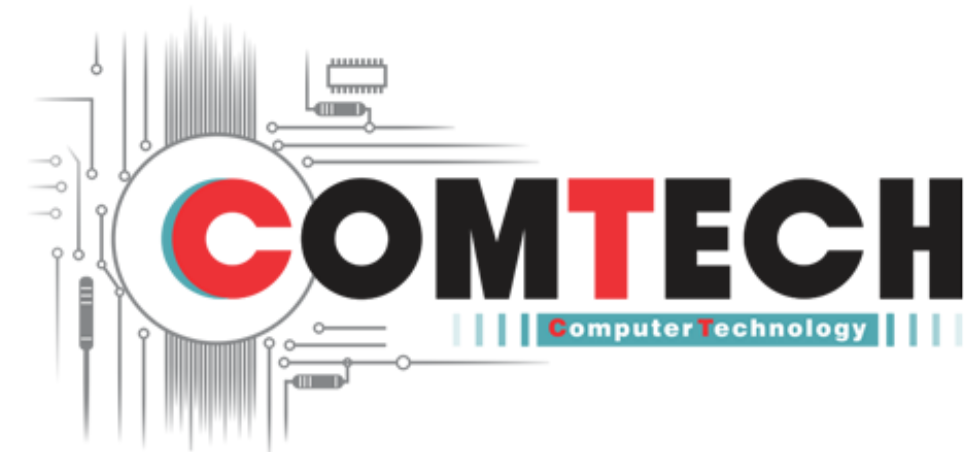
MSM8953 POWER2



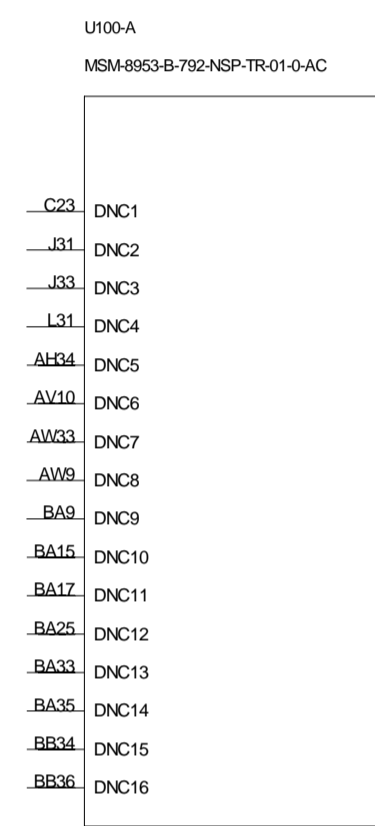
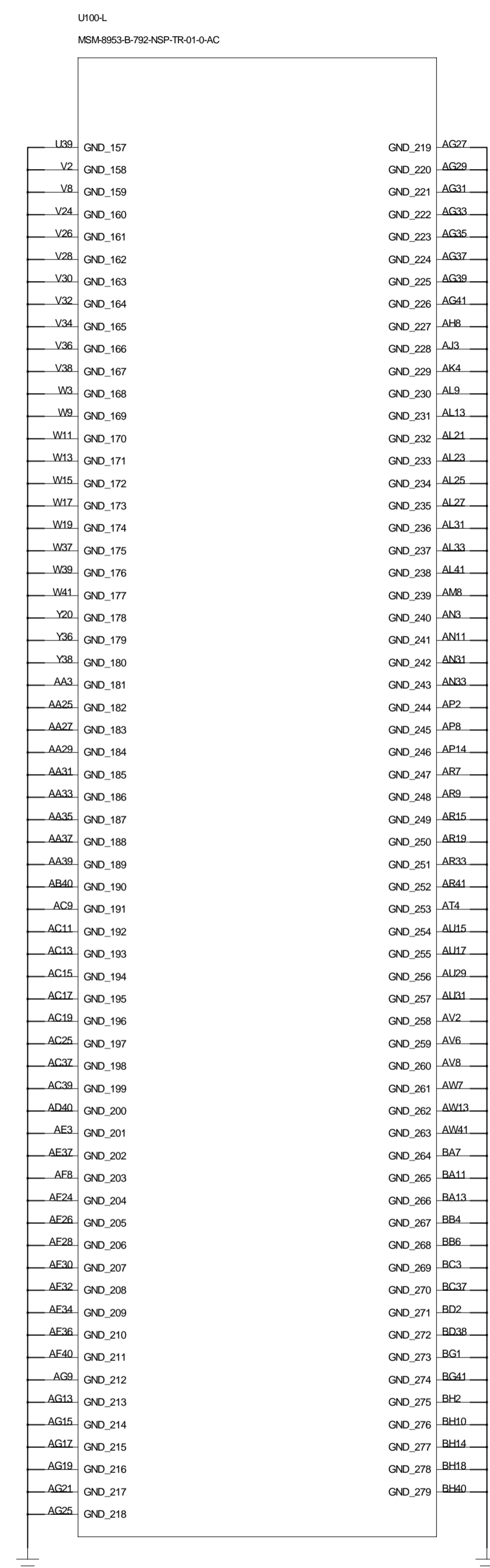
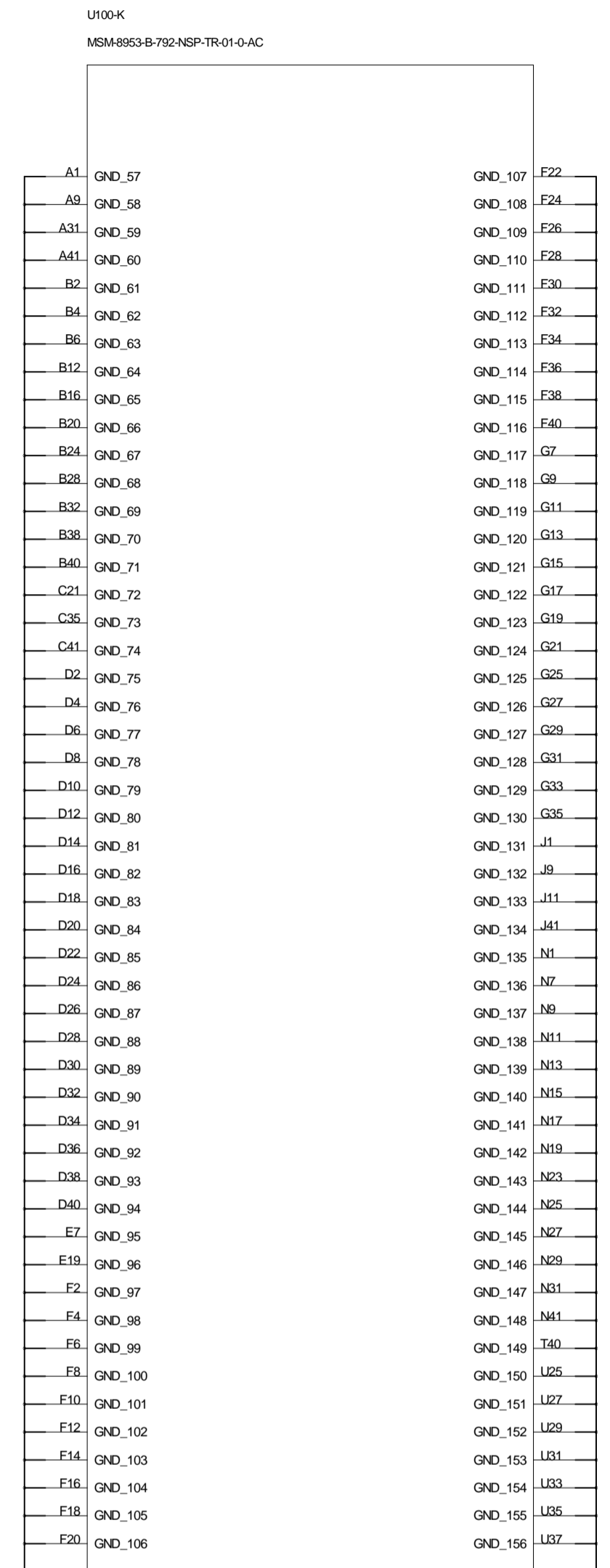
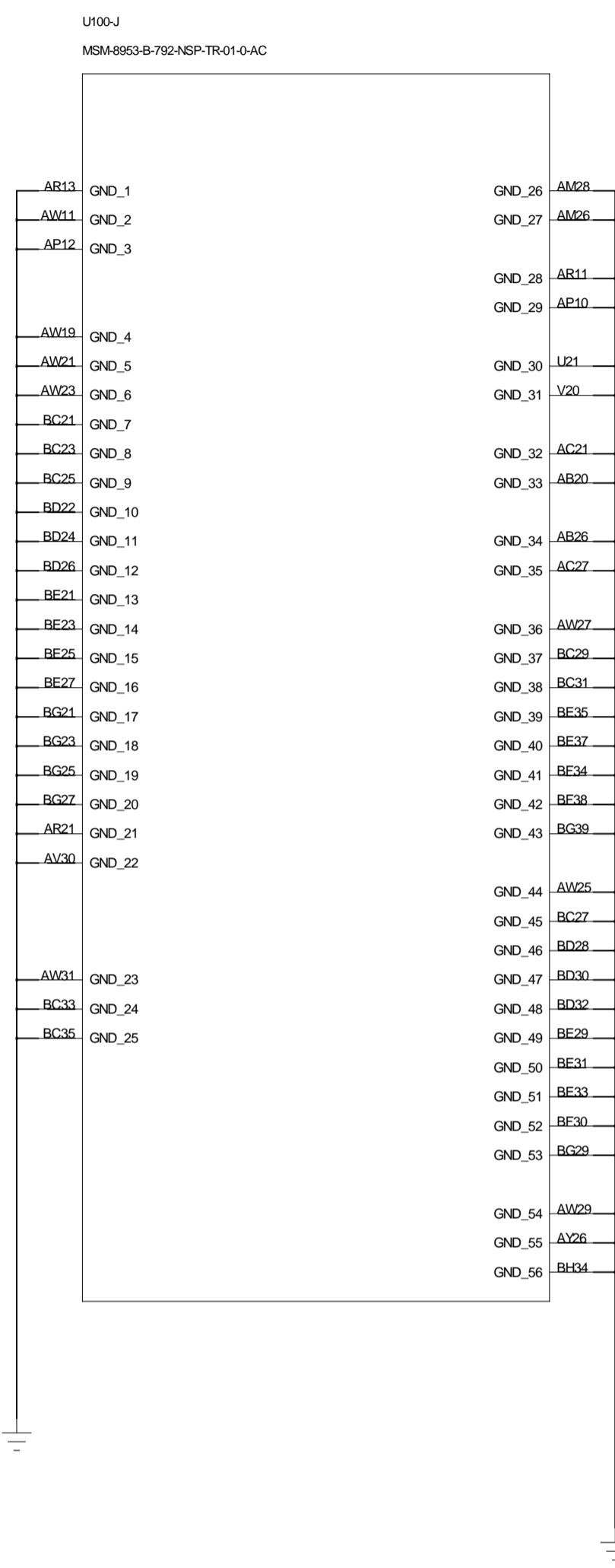
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MSM8953 GND

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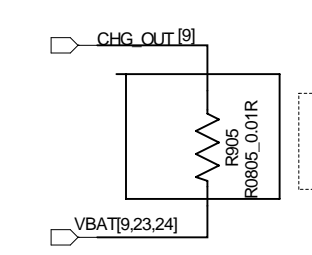
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PMI PIN	connection on device without Wipower	connection on device with Wipower
CHG_OK	Pull up to VDD_CAP with 5kohm	Stark PRU CHG_OK
DIV2_EN	Pull down to GND with 0ohm	Stark PRU DIV2_EN
GP102	No Connect	10Kohm pull down to gnd

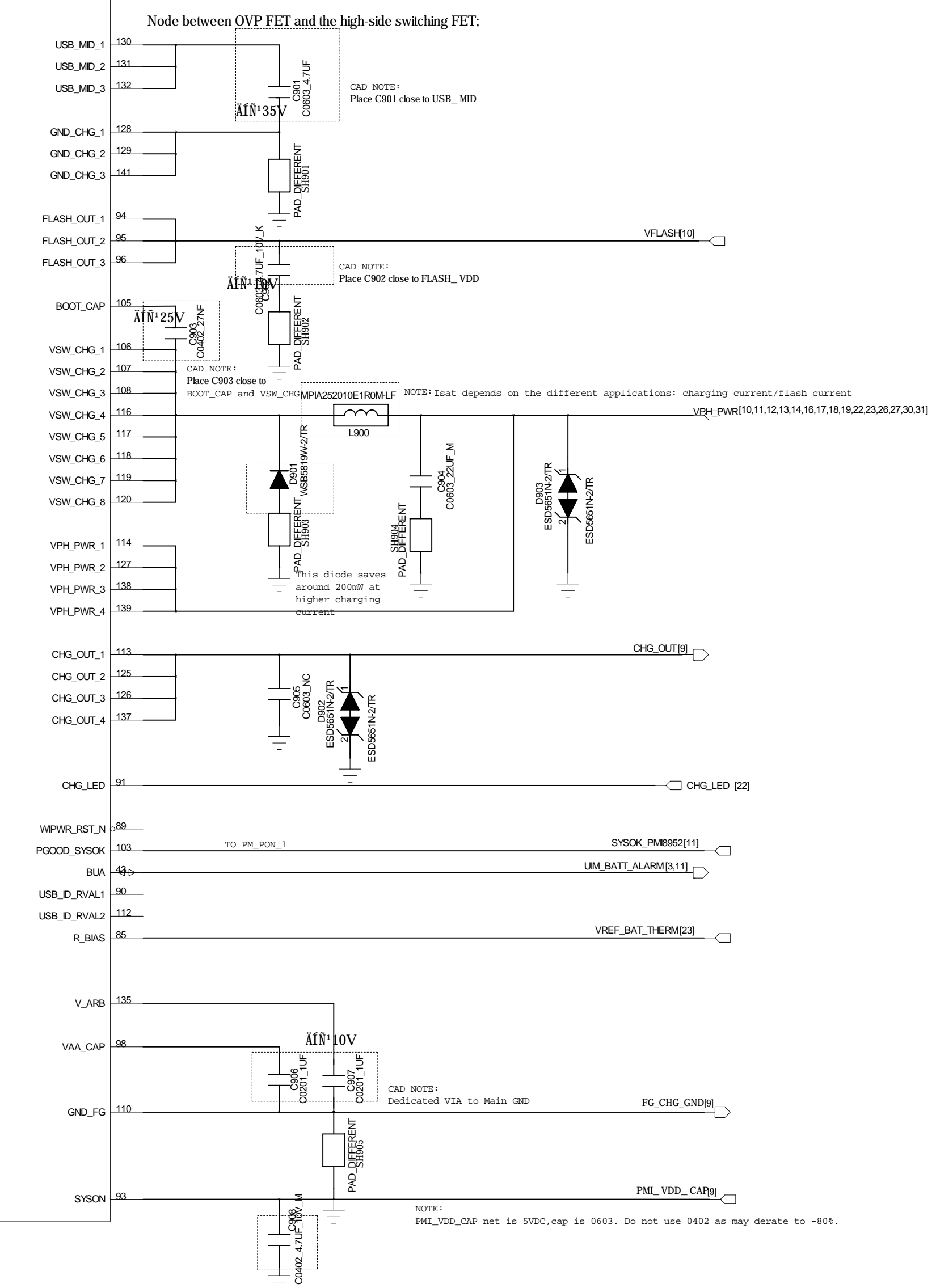
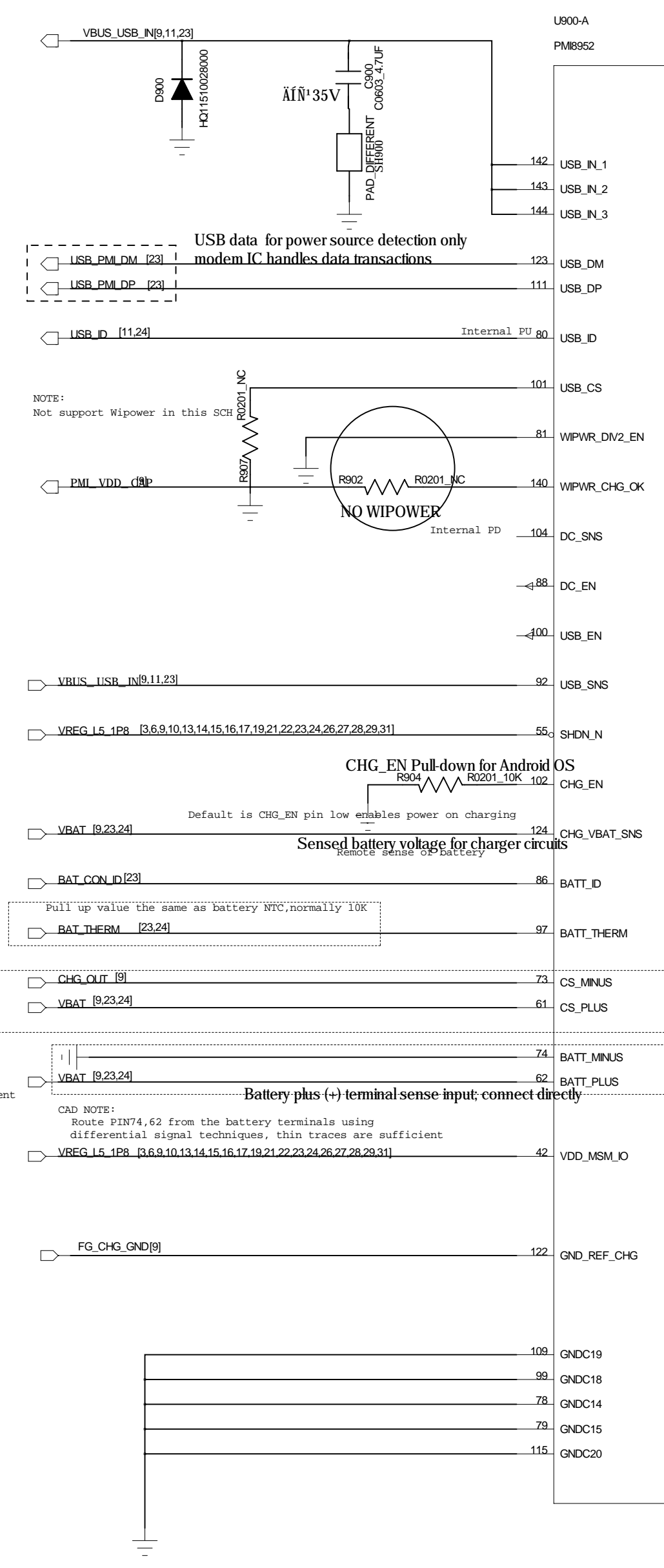
For parallel charging! Connects to SMB RN pin!
Do NOT pull up to VDD_CAP

For parallel charging! Connects to SMB RN pin!
Do NOT pull up to VDD_CAP

Close the Battery Connector:



CAD NOTE:
Route P1N73_61 from the sense resistor using differential signal techniques, this traces are sufficient

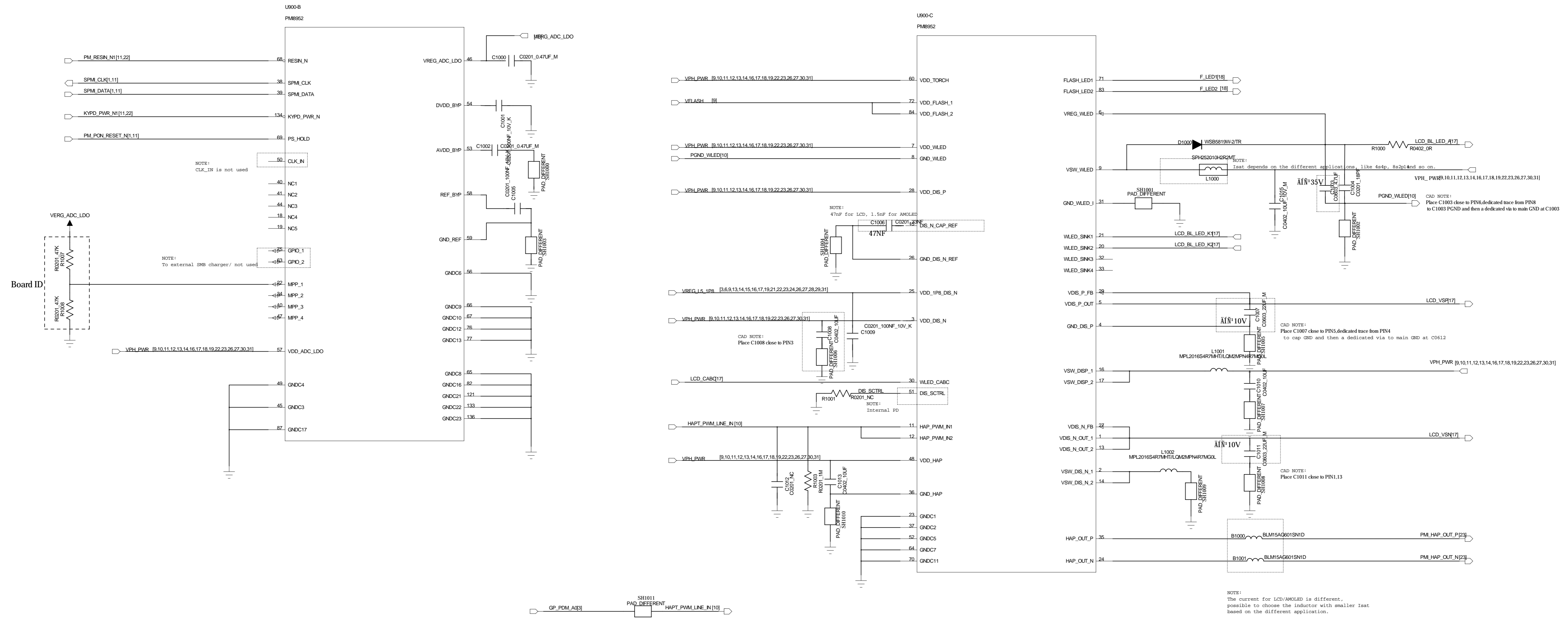


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PMI8952 Charger

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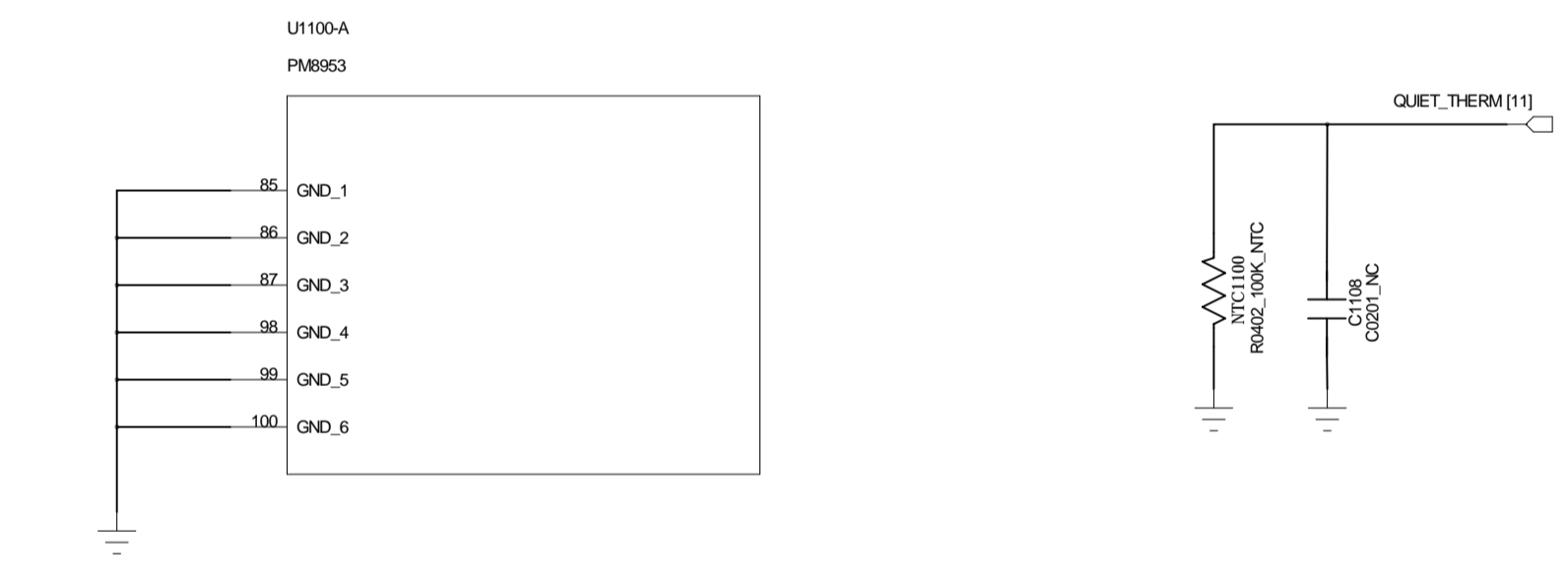
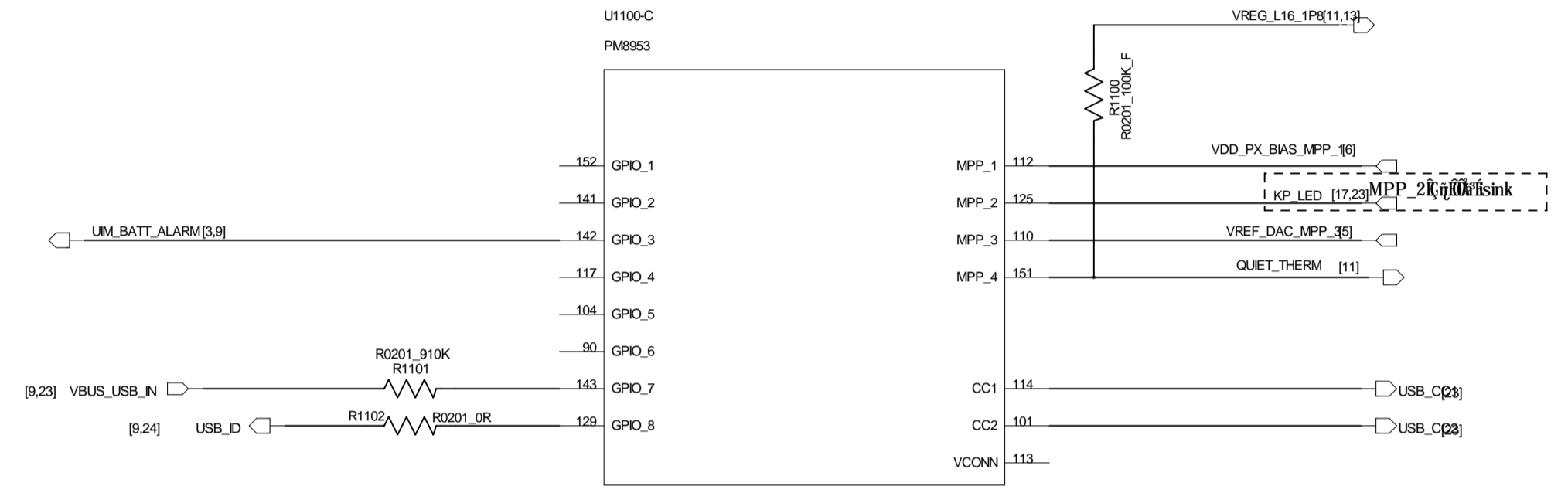
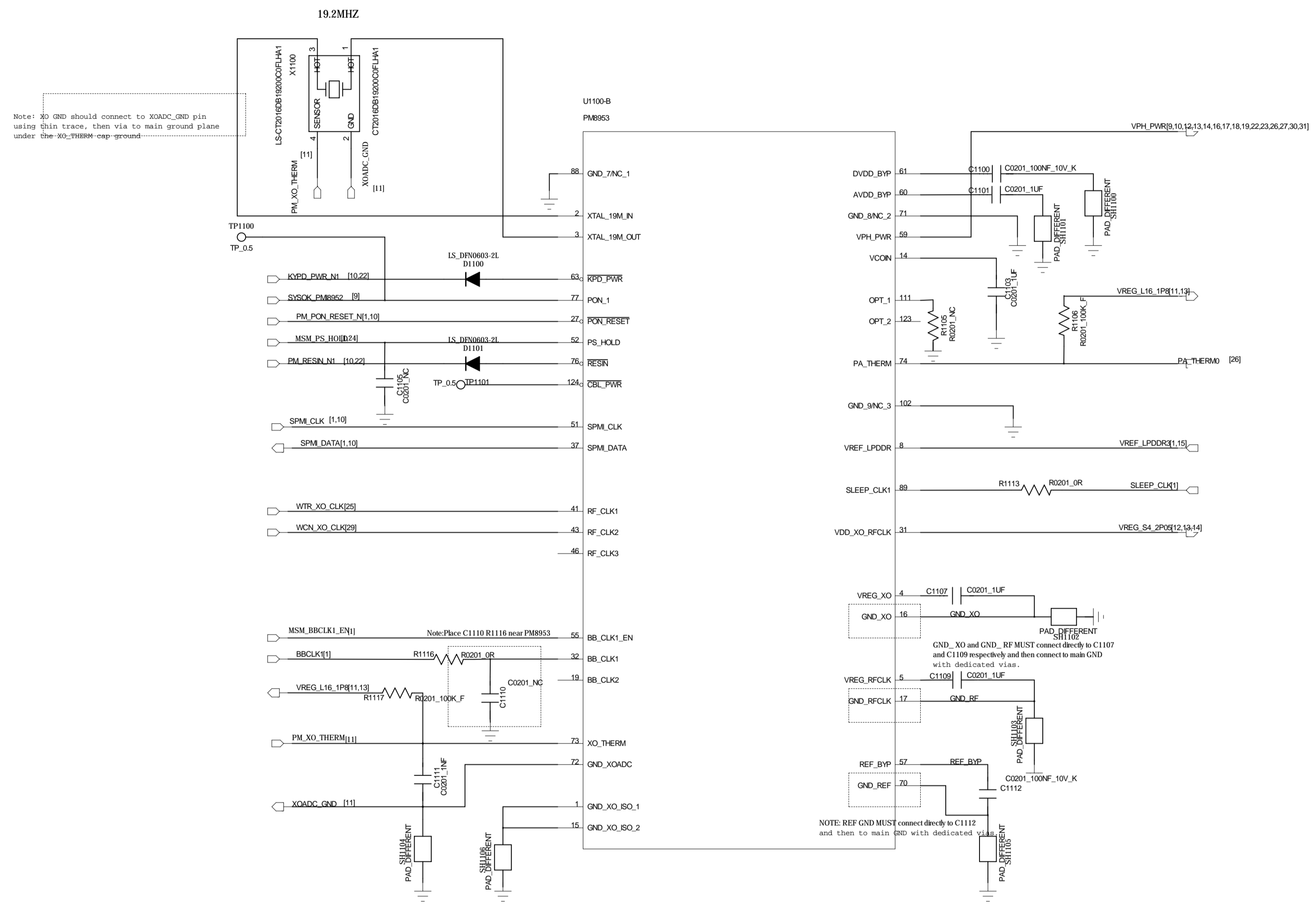


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PMI8952 Control/Interface

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Note: XO GND should connect to XOADC_GND pin using thin trace, then via to main ground plane under the XO_THERM cap ground.

NOTE: REF_GND MUST connect directly to C1112 and then to main GND with dedicated vias.

Note: Place C1110 R1116 near PM8953. GND_XO and GND_REF MUST connect directly to C1107 and C1109 respectively and then connect to main GND with dedicated vias.

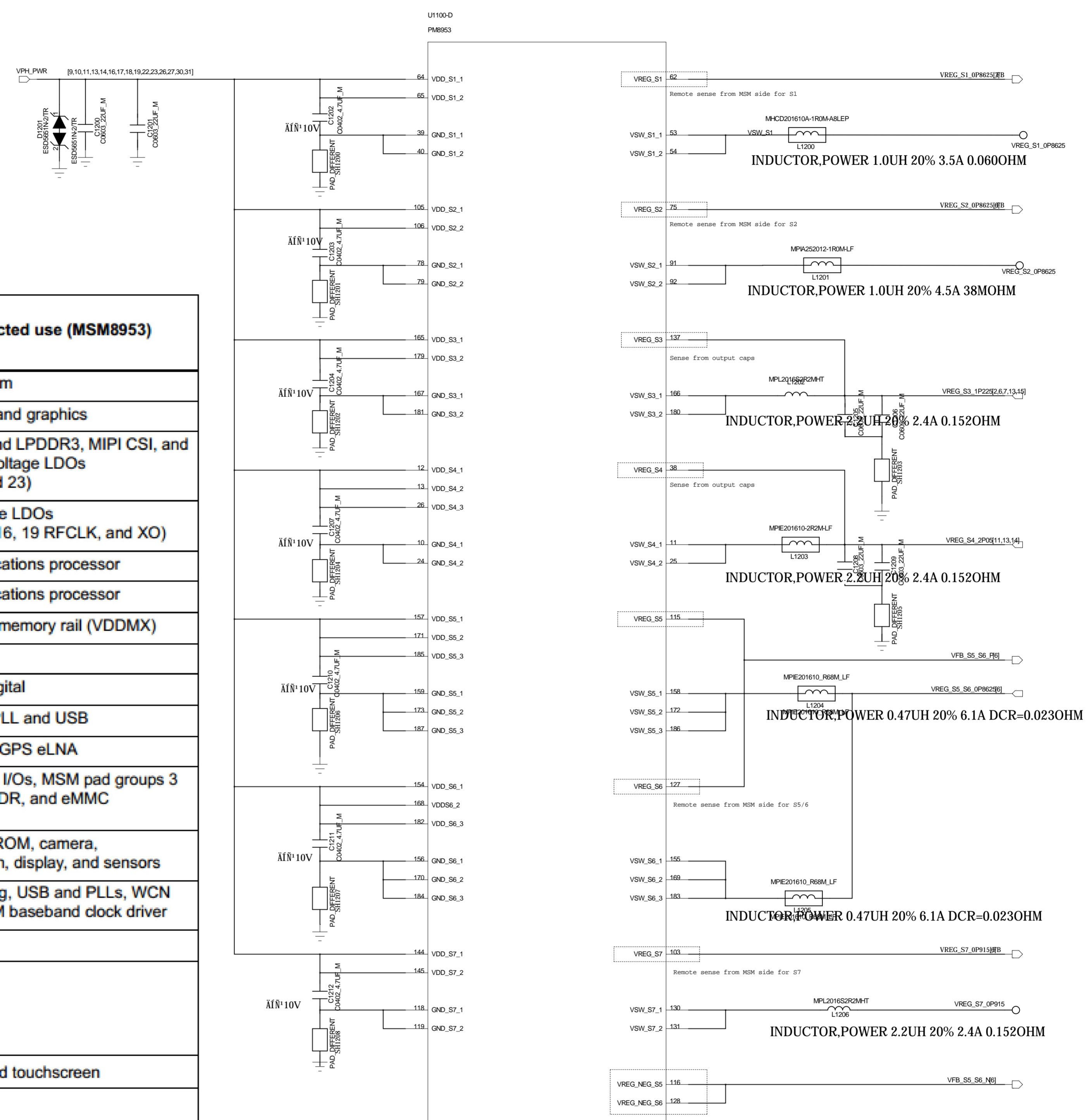
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PM8953 Control/Interface

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Function	Circuit type	Default voltage (V) ¹	Specified range (V) ² (MSM8953)	Programmable range (V)	Rated current (mA)	Default on	Expected use (MSM8953)
S1	SMPS	0.87	0.4–1.14	0.32–2.04	3000	N	MSM modem
S2	SMPS	0.87	0.4–1.14	0.32–2.04	4000	Y	MSM core and graphics
S3	SMPS	1.225	1.2–1.25	0.32–2.04	2000	Y	LPDDR2 and LPDDR3, MIPI CSI, and DSI. Low-voltage LDOs (1, 2, 3, and 23)
S4	SMPS	2.04	1.2–1.25	0.32–2.04	2000	Y	High-voltage LDOs (4, 5, 6, 7, 16, 19 RFCLK, and XO)
S5	SMPS	0.87	0.4–1.14	0.350–1.355	3750	Y	MSM applications processor
S6	SMPS	0.87	0.4–1.14	0.350–1.355	3750	Y	MSM applications processor
S7	SMPS	0.915	0.900-1.350V	0.375–1.5625	2000	Y	MSM VDD memory rail (VDDMX)
L1	NMOS LDO	1.000	1.000	0.375–1.5375	600	N	RFICs
L2	NMOS LDO	1.100	1.100	0.375–1.5375	1200	Y	Camera: digital
L3	NMOS LDO	0.925	0.925	0.375–1.5375	600	Y	MSM DSI PLL and USB
L4	PMOS LDO	1.800	1.800	1.750–3.3375	450	N	RFICs and GPS eLNA
L5 ³	PMOS LDO	1.800	1.800	1.750–3.3375	600	Y	Most digital I/Os, MSM pad groups 3 and 7, LPDDR, and eMMC
L6	PMOS LDO	1.800	1.800	1.750–3.3375	300	N	MSM QFPROM, camera, touchscreen, display, and sensors
L7	PMOS LDO	1.800	1.800	1.750–3.3375	300	Y	MSM analog, USB and PLLs, WCN XO, and PM baseband clock driver
L8	PMOS LDO	2.900	2.900	1.750–3.3375	600	Y	eMMC
L9	PMOS LDO	$V_{out} = 3.3\text{ V}$ for $V_{BAT} > 3.575\text{ V}$; $V_{out} = 3\text{ V}$ for $V_{BAT} < 3.575\text{ V}$	3.000–3.300	1.750–3.3375	600	N	WCN
L10	PMOS LDO	3.0	3.0	1.750–3.3375	150	N	Sensors and touchscreen
L11 ⁴	PMOS LDO	2.950	2.950	1.750–3.3375	800	Y	Micro SD



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PM8953 SMPS



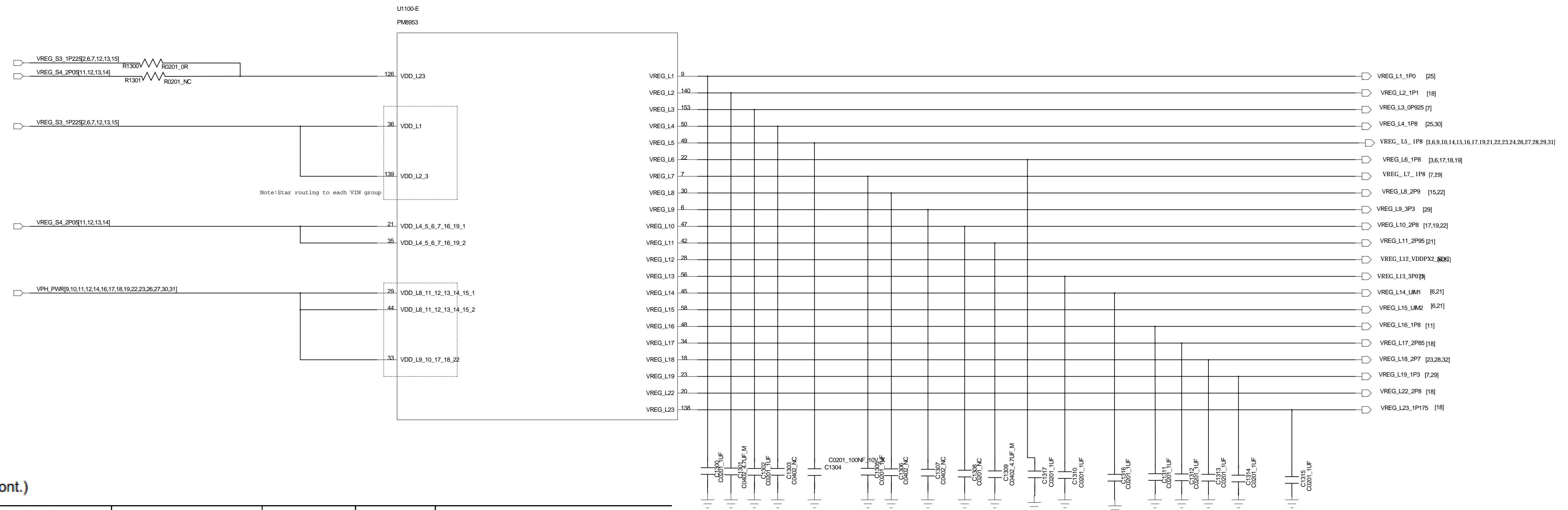


Table 3-7 PM8953 regulators and their intended uses (cont.)

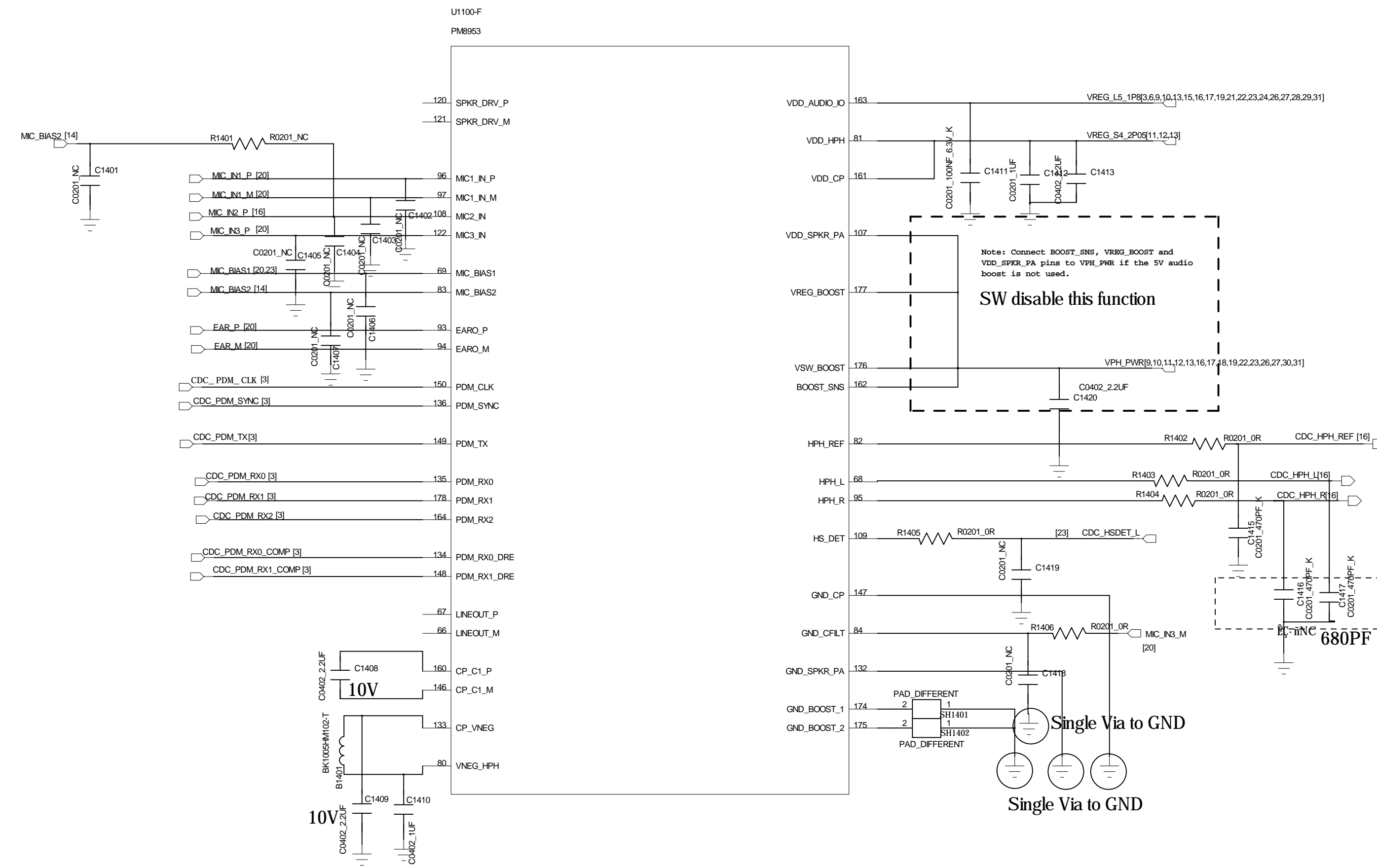
Function	Circuit type	Default voltage (V) ¹	Specified range (V) ² (MSM8953)	Programmable range (V)	Rated current (mA)	Default on	Expected use (MSM8953)
L12 ³	PMOS LDO	2.950	1.800/2.950	1.750–3.3375	50	Y	MSM pad group 2
L13	PMOS LDO	3.125	3.125	1.750–3.3375	150	Y	MSM USB and PMIC and external codec audio
L14 ⁴	PMOS LDO	1.800	1.800/3	1.750–3.3375	50	N	MSM pad group 5, dual-voltage UIM1, and NFC
L15 ⁴	PMOS LDO	1.800	1.800/3	1.750–3.3375	50	N	MSM pad group 6 and dual-voltage UIM2
L16	PMOS LDO	1.800	1.800	1.750–3.3375	5	N	PMIC HKADC
L17	PMOS LDO	2.850	2.850	1.750–3.3375	300	N	Camera and display
L18	PMOS LDO	2.700	2.700	1.750–3.3375	150	N	QTI RF front-end
L19	NMOS LDO	1.350	1.350	0.375–1.5375	600	N	MSM analog, WCN, and WGR
L20	Low-noise LDO	1.74	1.74	1.74–3.3375	5	Y	PMIC XO circuits
L21	Low-noise LDO	1.74	1.74	1.74–3.3375	5	Y	PMIC RF clock buffers
L22	PMOS LDO	2.800	2.800	1.750–3.3375	150	N	Camera: analog
L23	NMOS LDO	1.15	1.15	0.375–1.5375	600	N	Camera: digital

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PM8953 LDO

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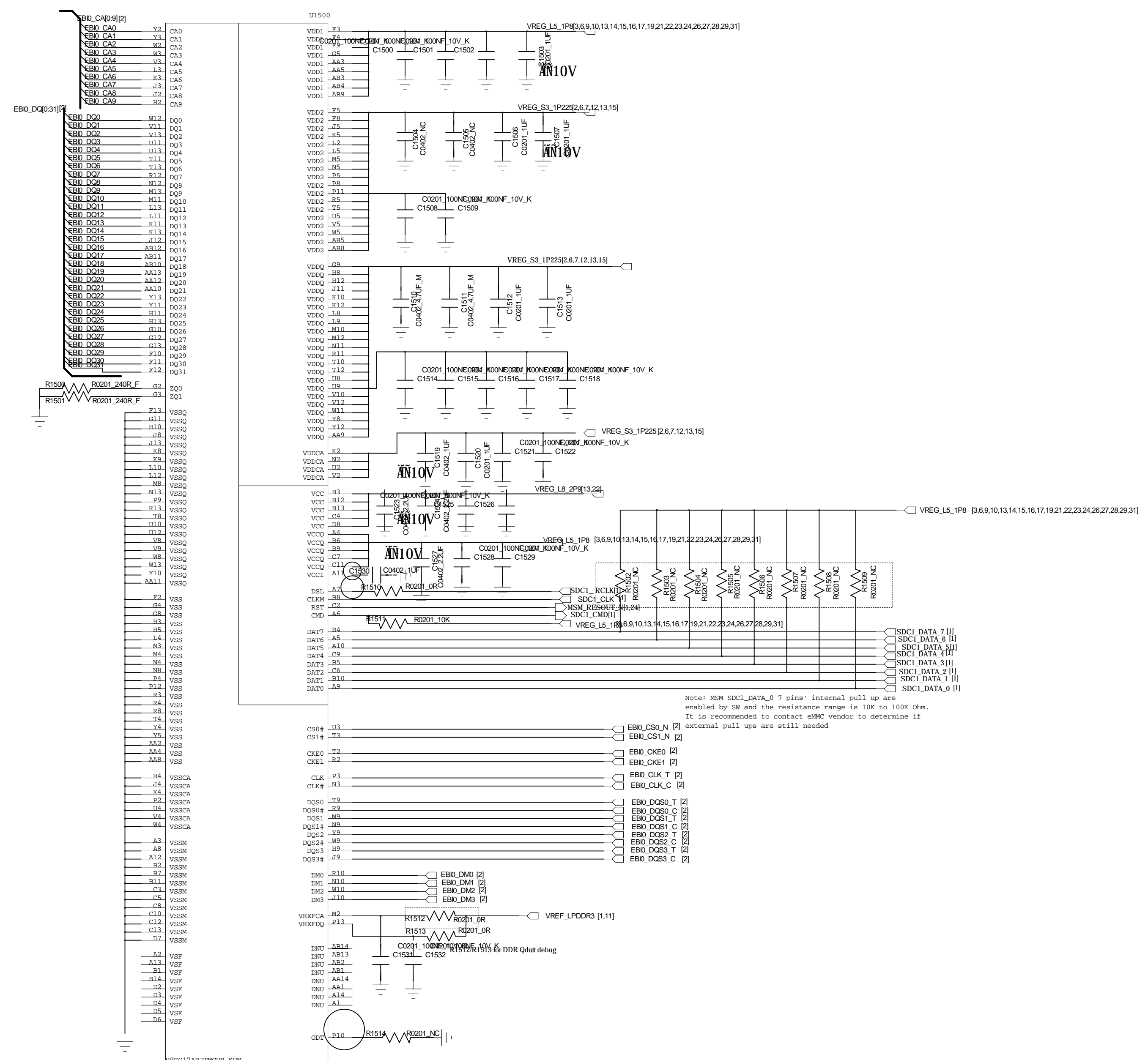
PM8953 CODEC/Audio PA

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Note: Follow the memory vendor recommendations on decoupling capacitor configuration.

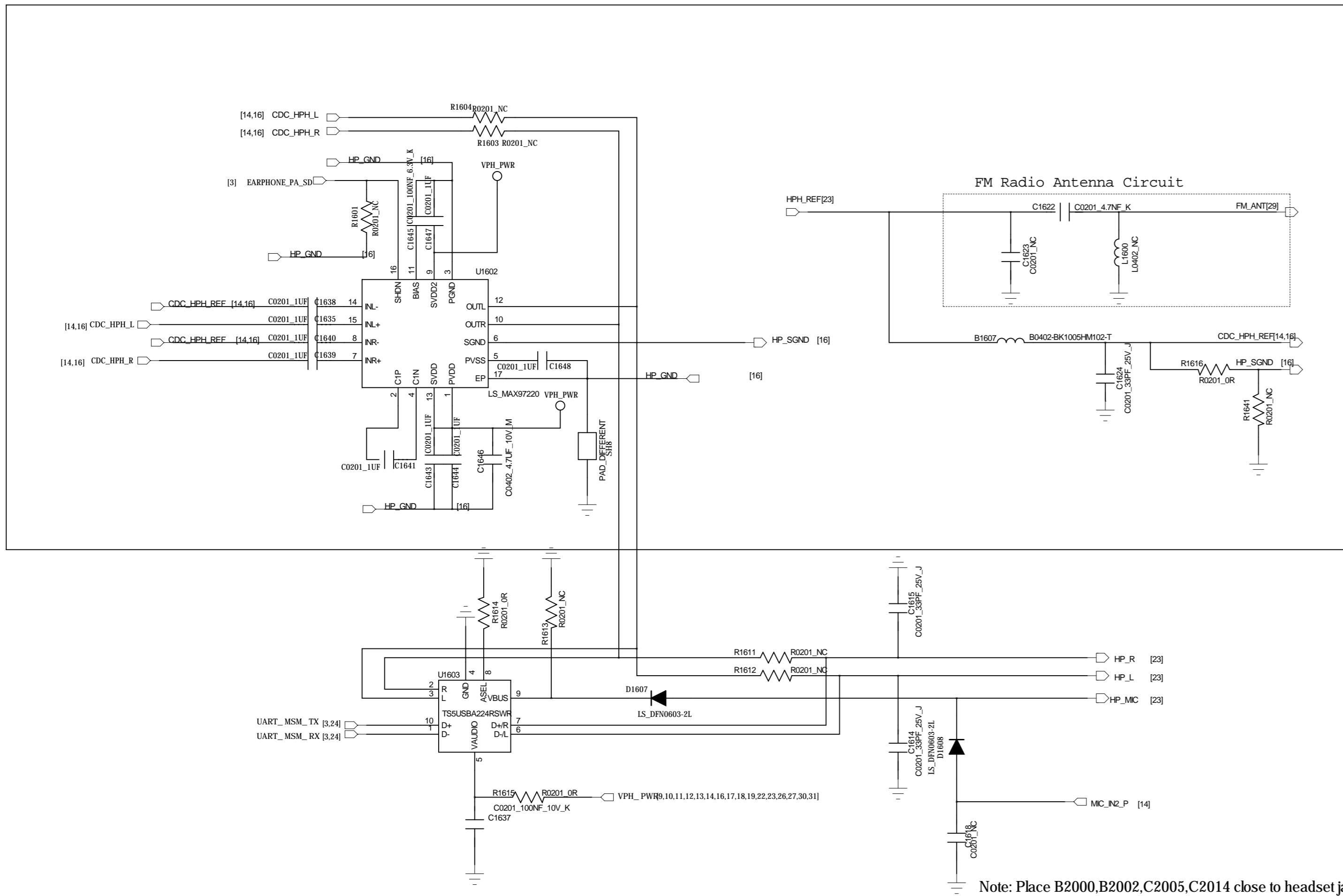
Please contact with memory vendor to get the PDR spec for LPDDR power rail.

Note: MSM SDC1_DATA_0-7 pins' internal pull-up are enabled by SM and the resistance range is 10K to 100K Ohm. It is recommended to contact OEM vendor to determine if external pull-ups are still needed.

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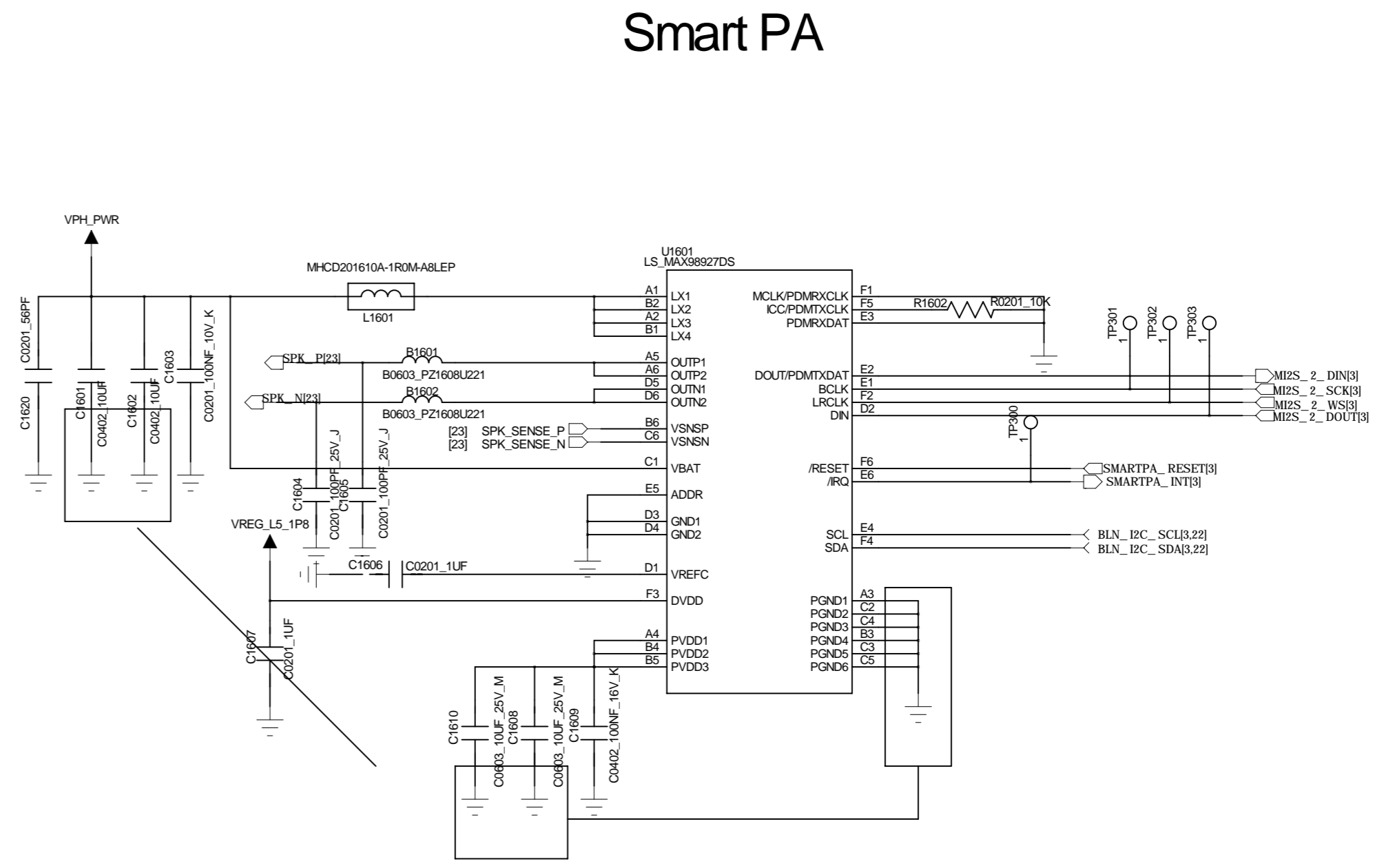
MEMORY(LPDDR3+EMMC V5.1

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Title Sheet Size Name Date: 1 Sheet of	



Note: Place B2000,B2002,C2005,C2014 close to headset jack connector

Note: Ferrite beads and their corresponding bypass capacitors on CDC_HPH_L_P, CDC_HPH_L_M and CDC_HPH_REF are needed to reduce noise generated by audio/FM concurrency

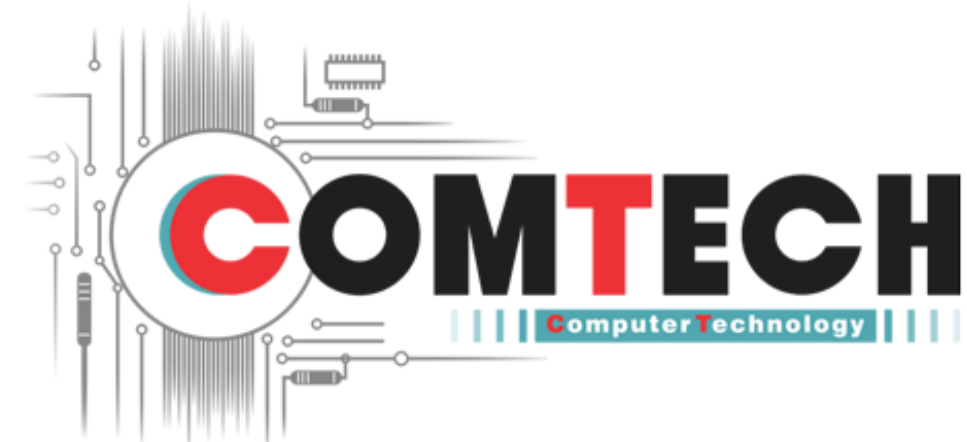


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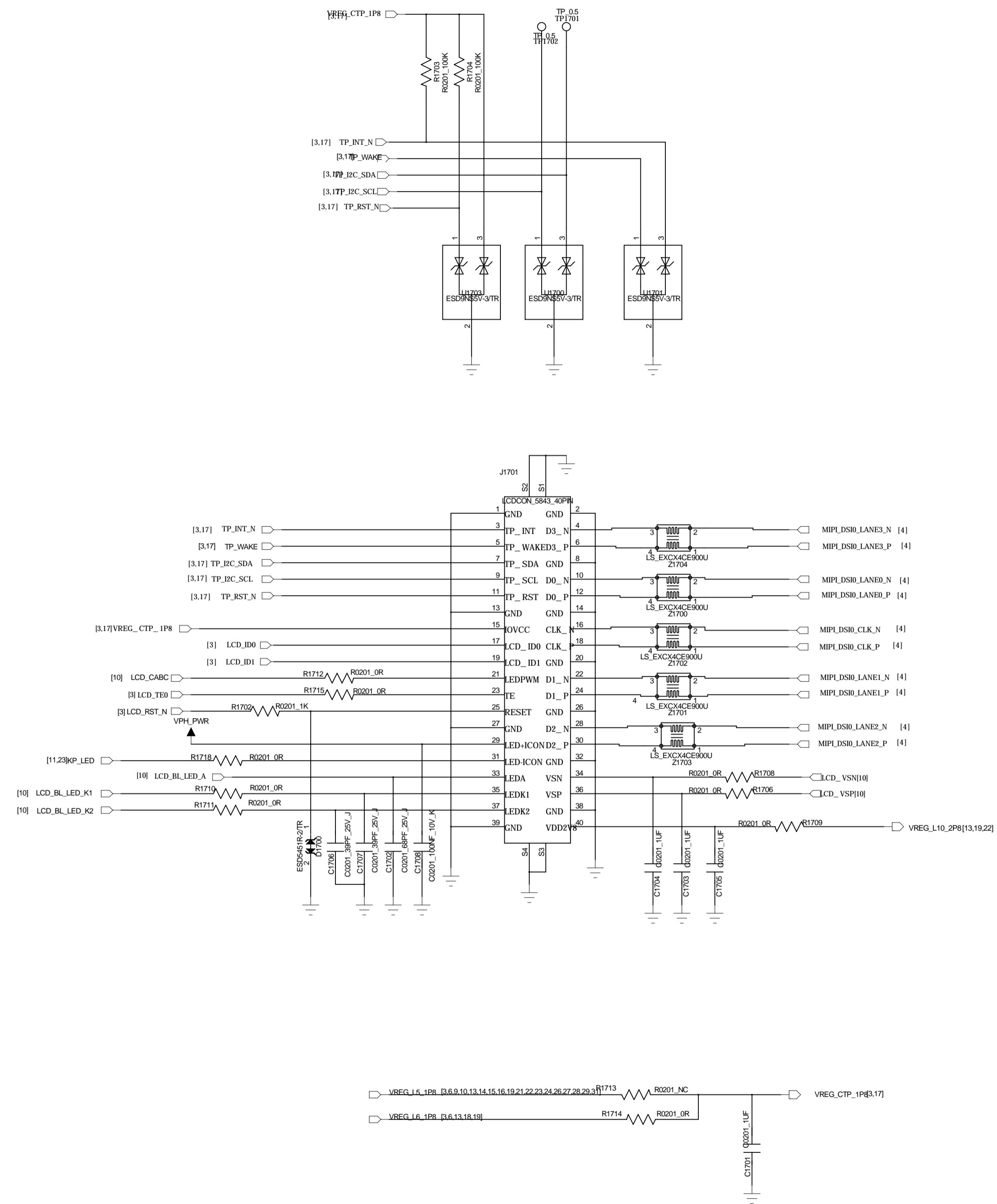
WCD9326 CODEC

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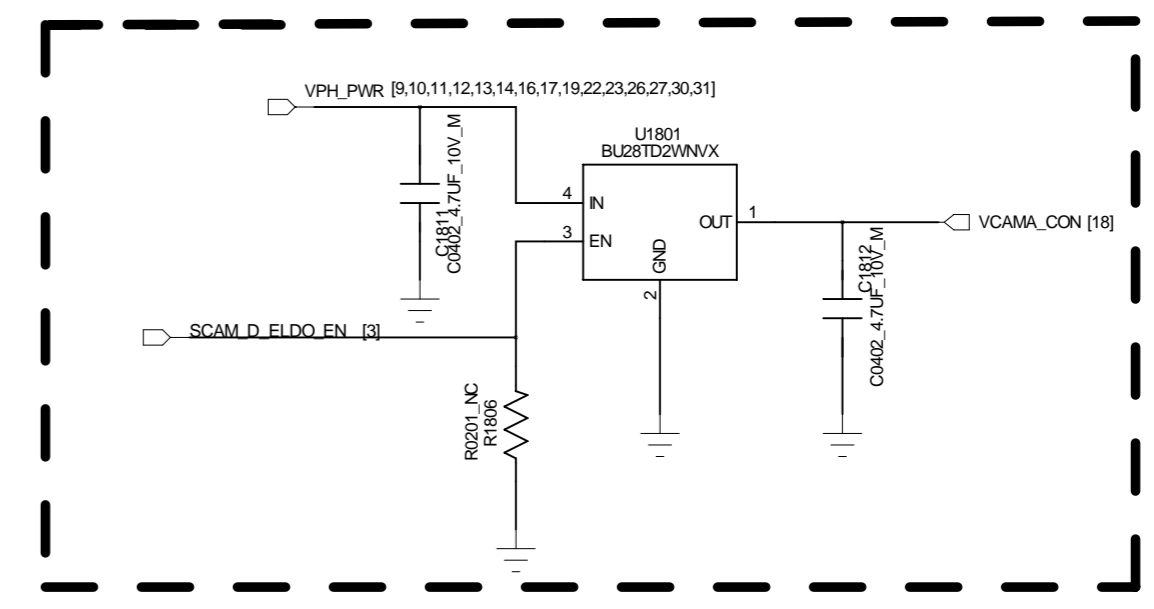
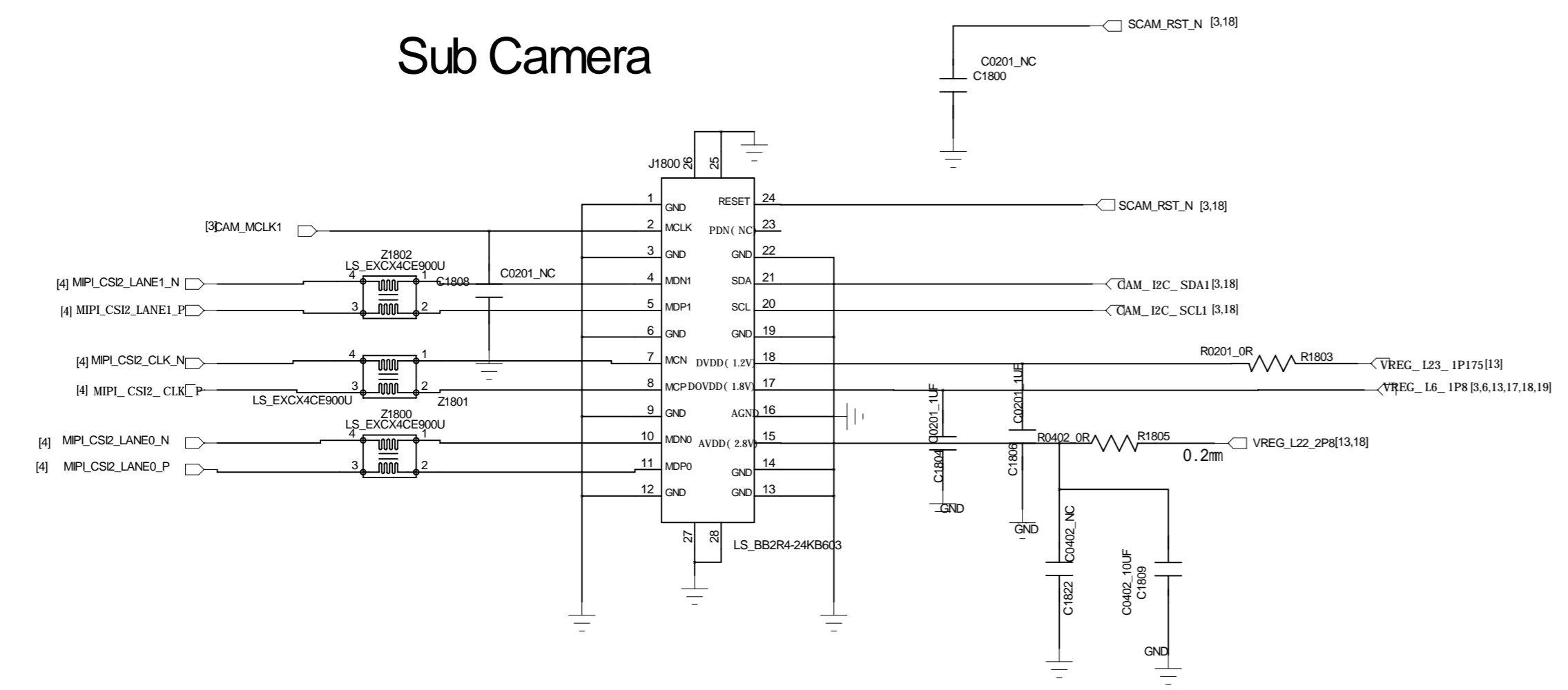
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LCD/CTP

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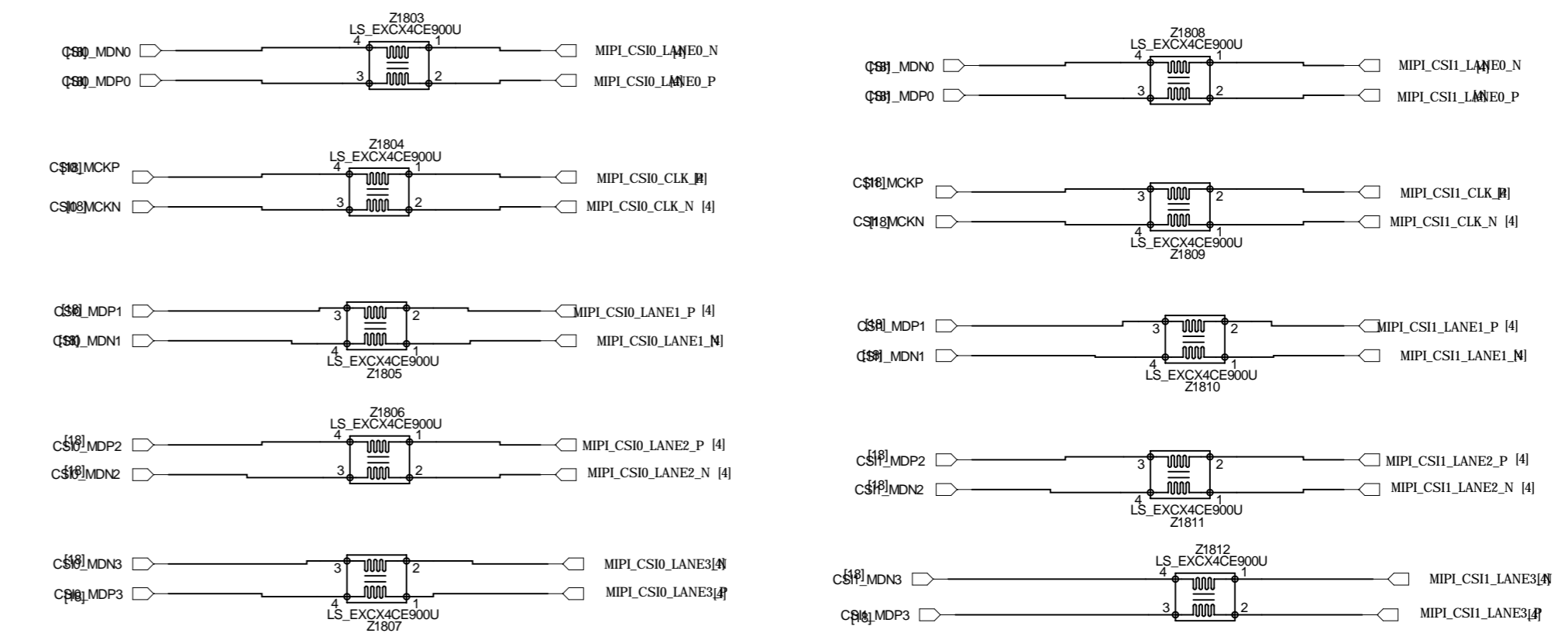
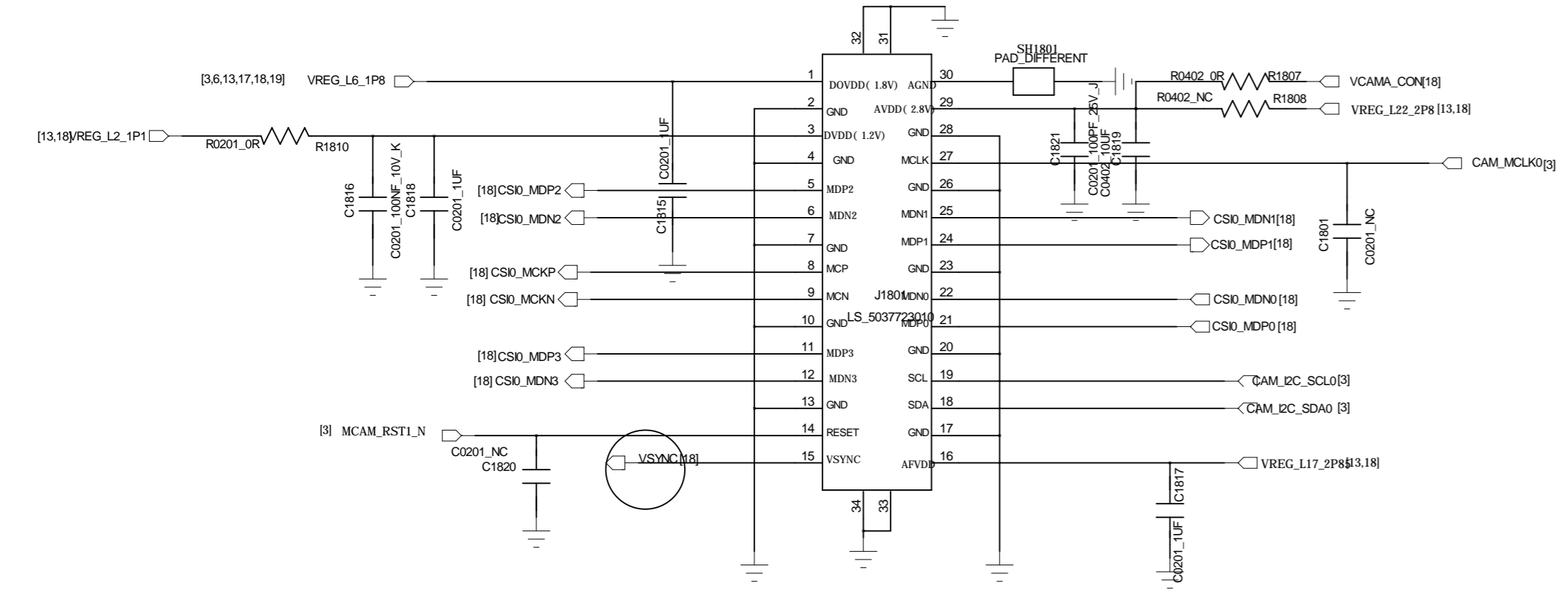
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Sub Camera

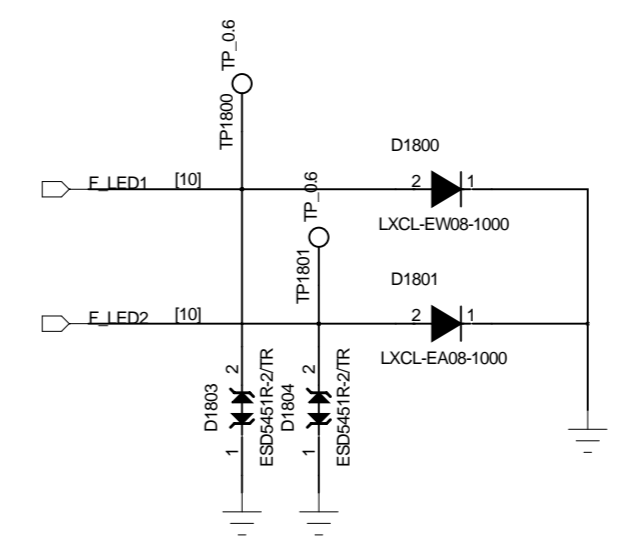
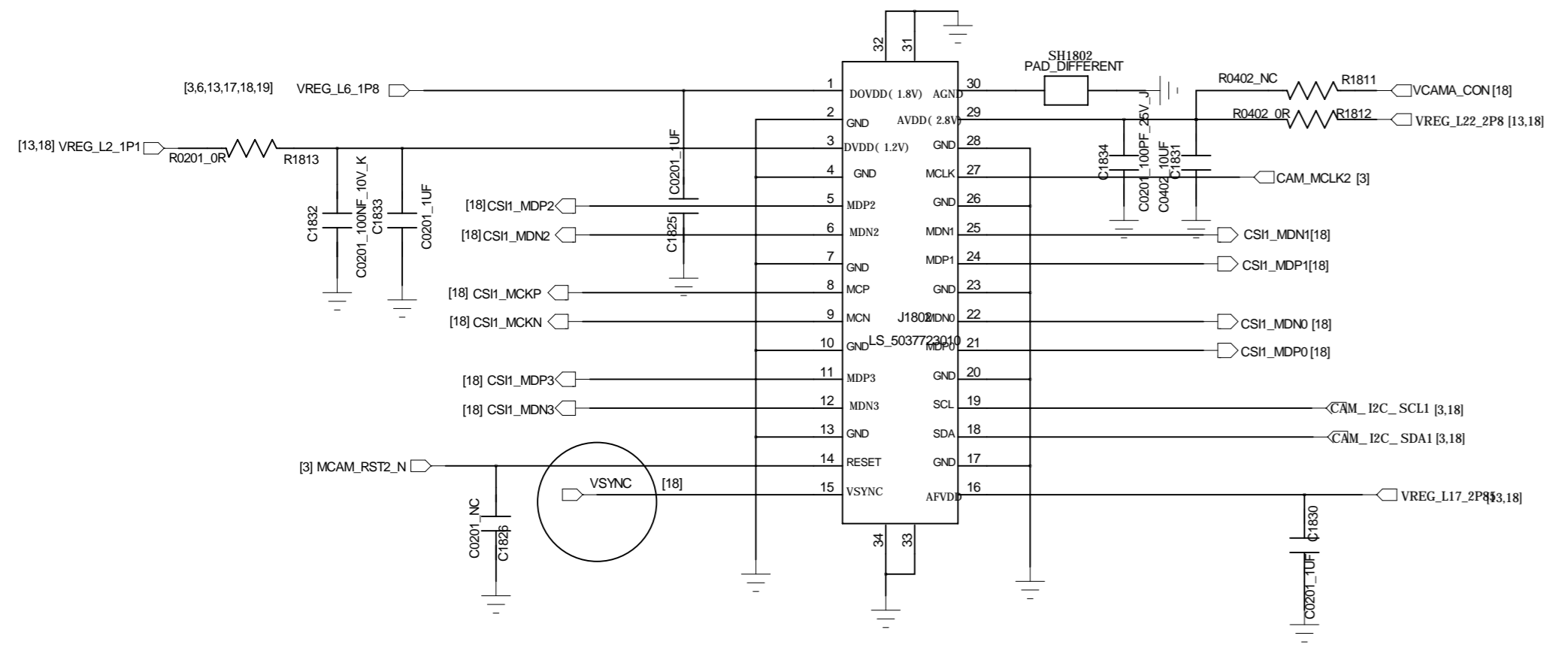


Main CAMERA

Master



Slave

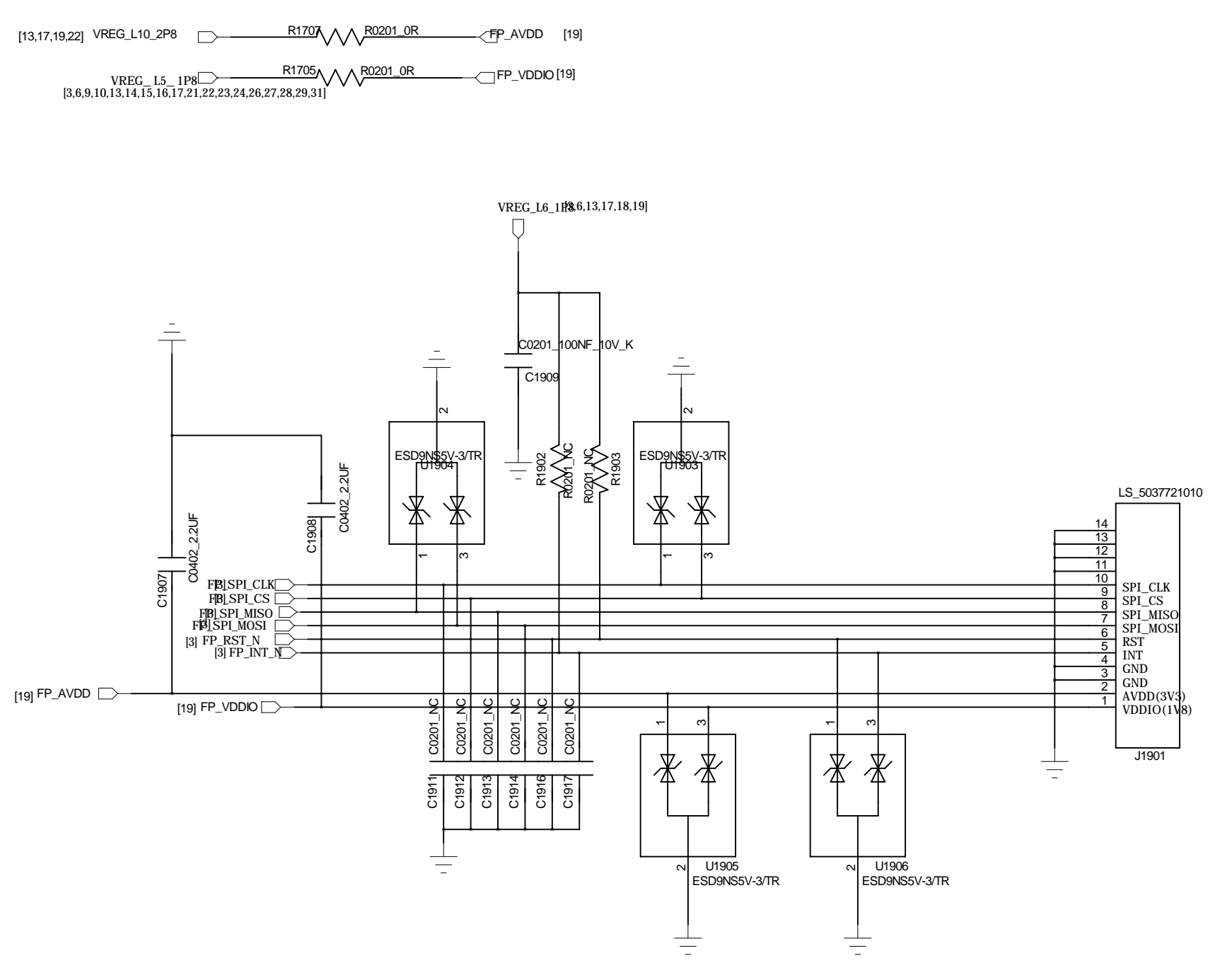
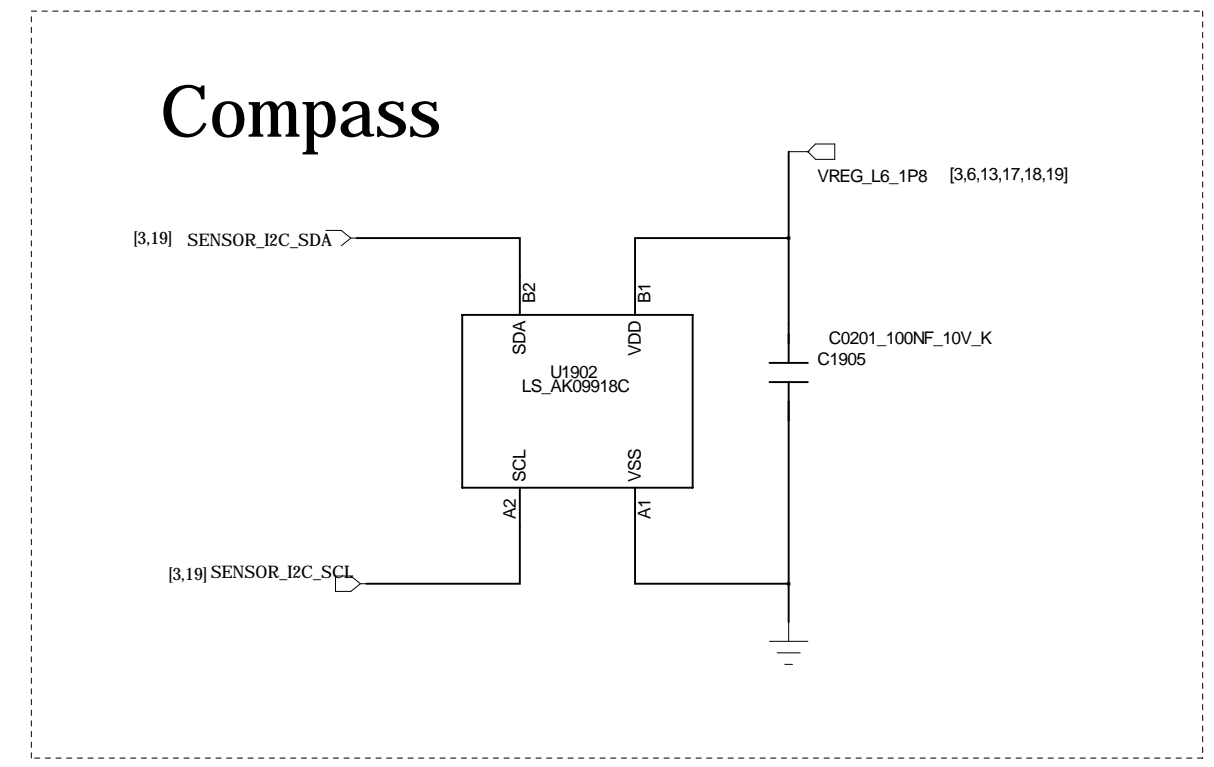
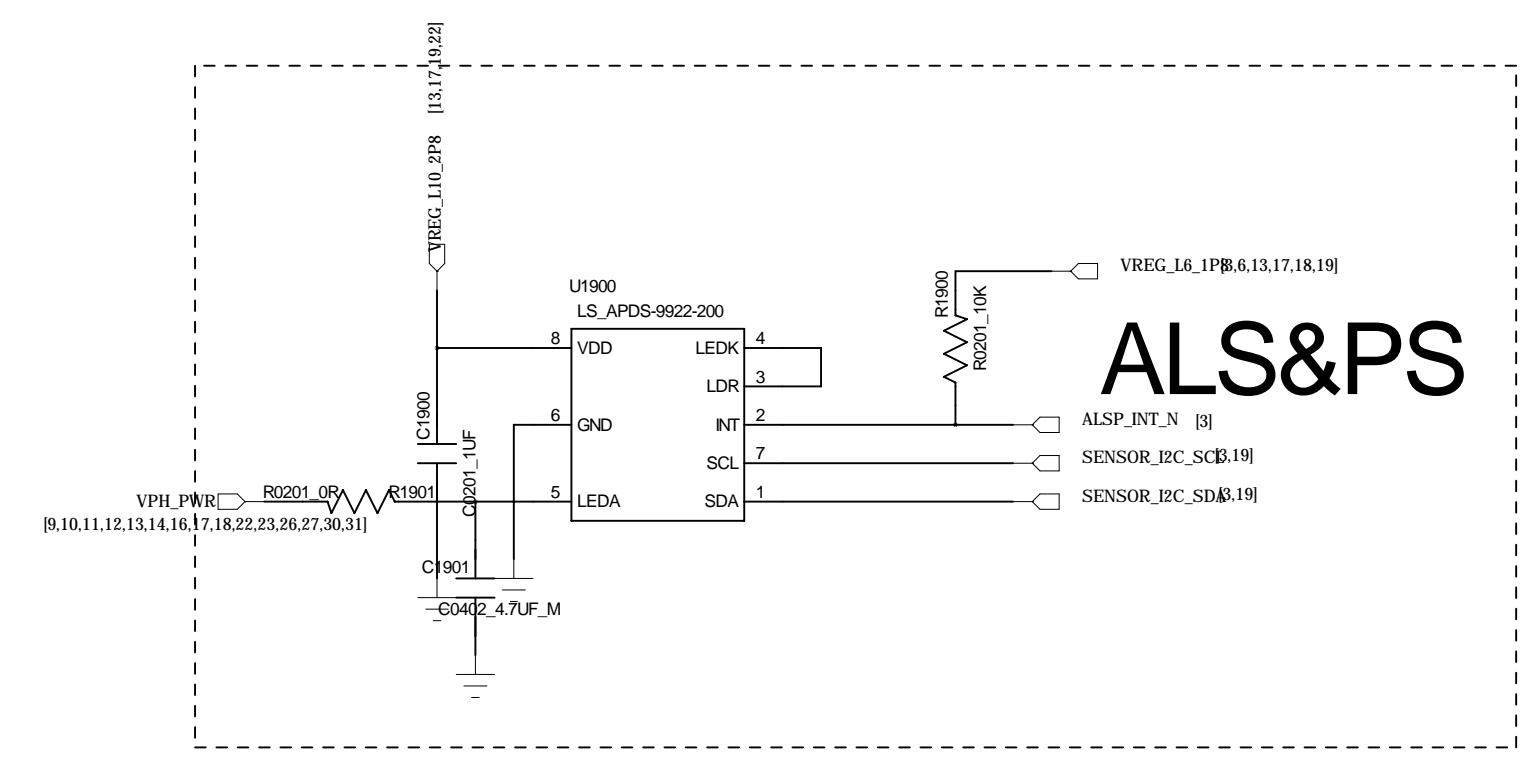
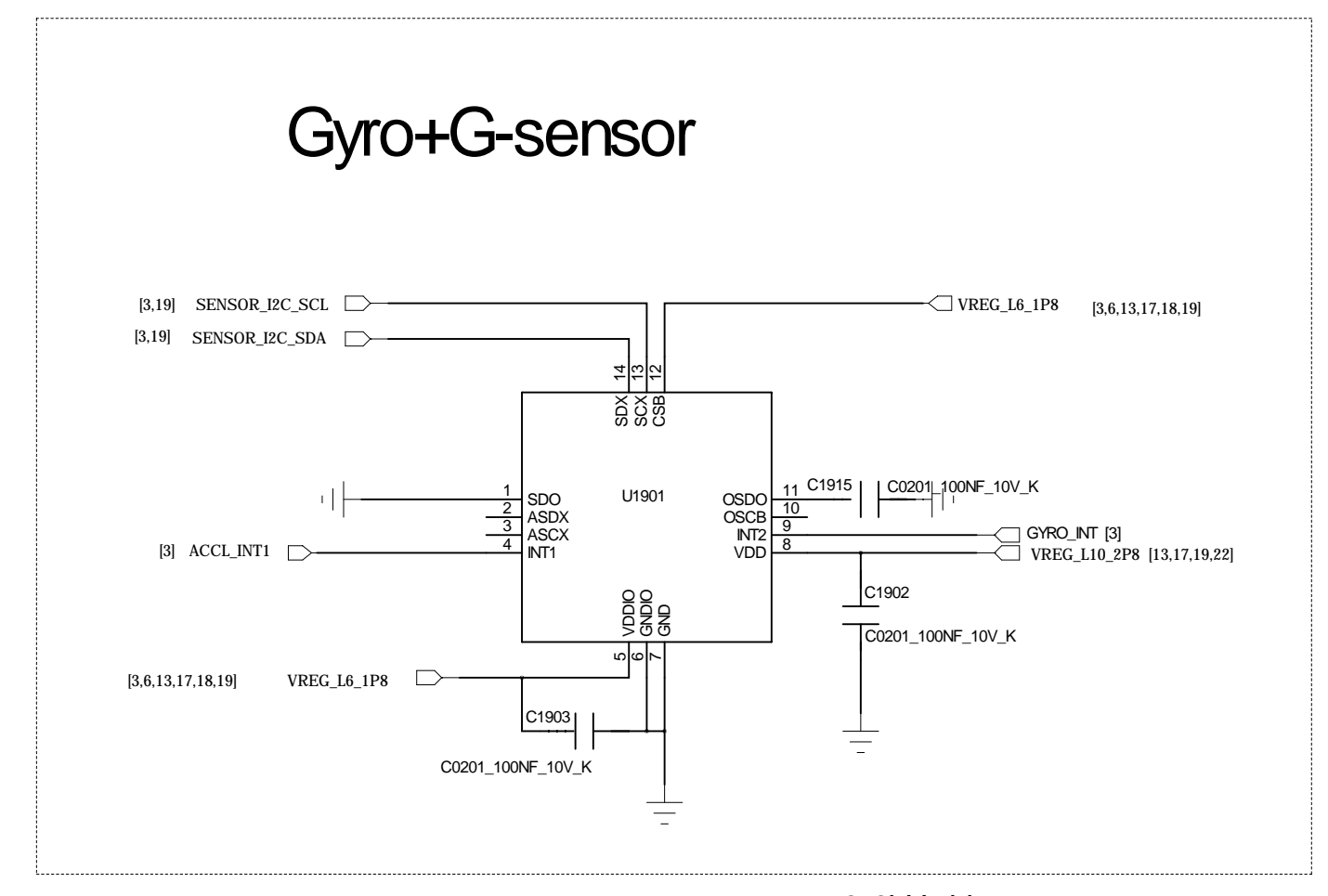


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Camera/Flash

VANA and VDIG and VIF may rise in any order

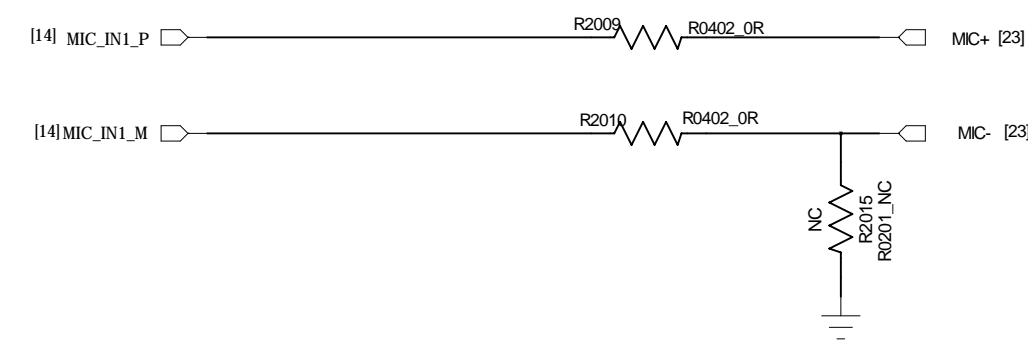
Sensor I2C addr:x020
Driver IC I2C addr:0xE4



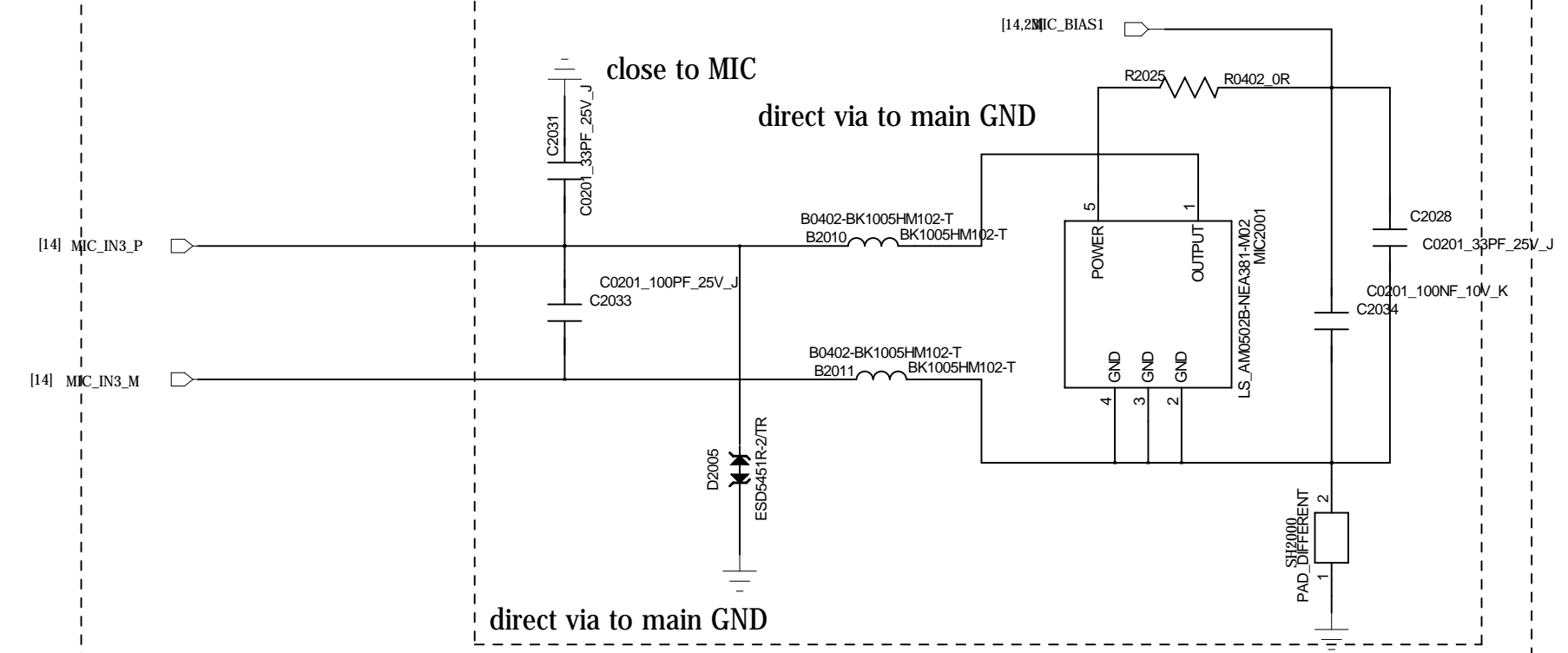
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Sensor

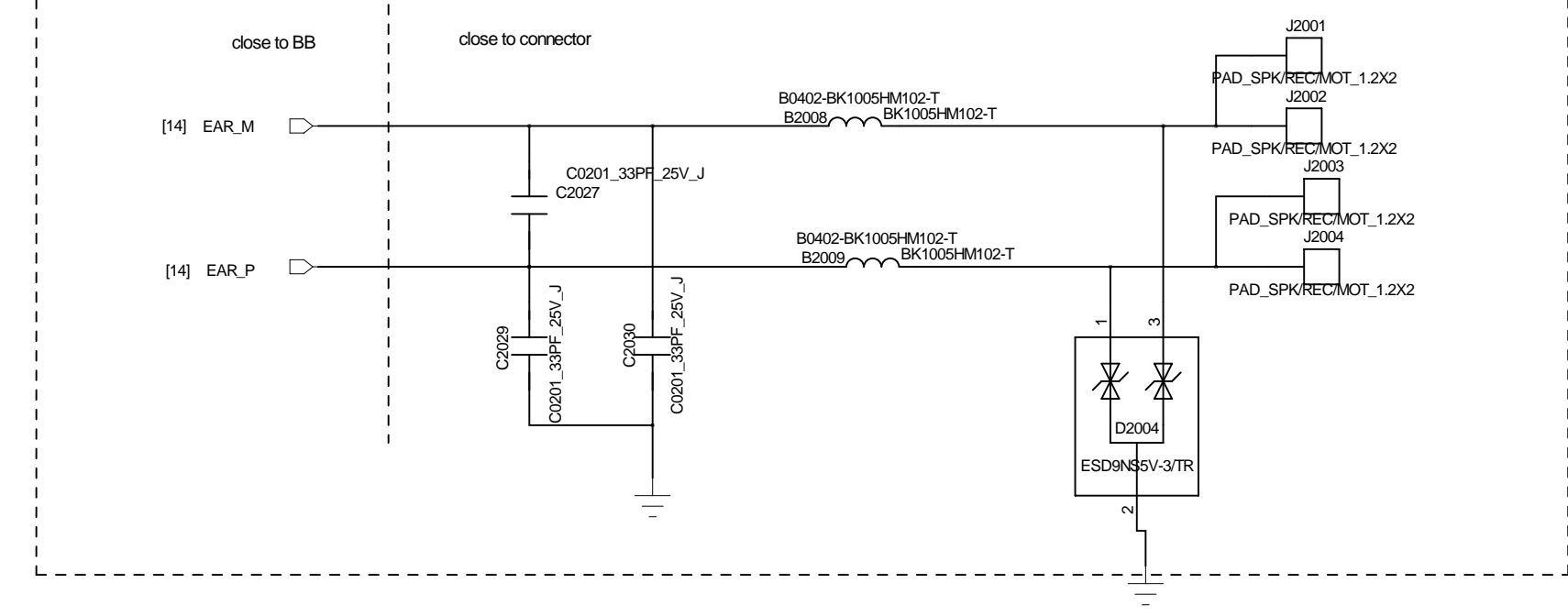
MIC -- Main



MIC -- Sub



RECEIVER

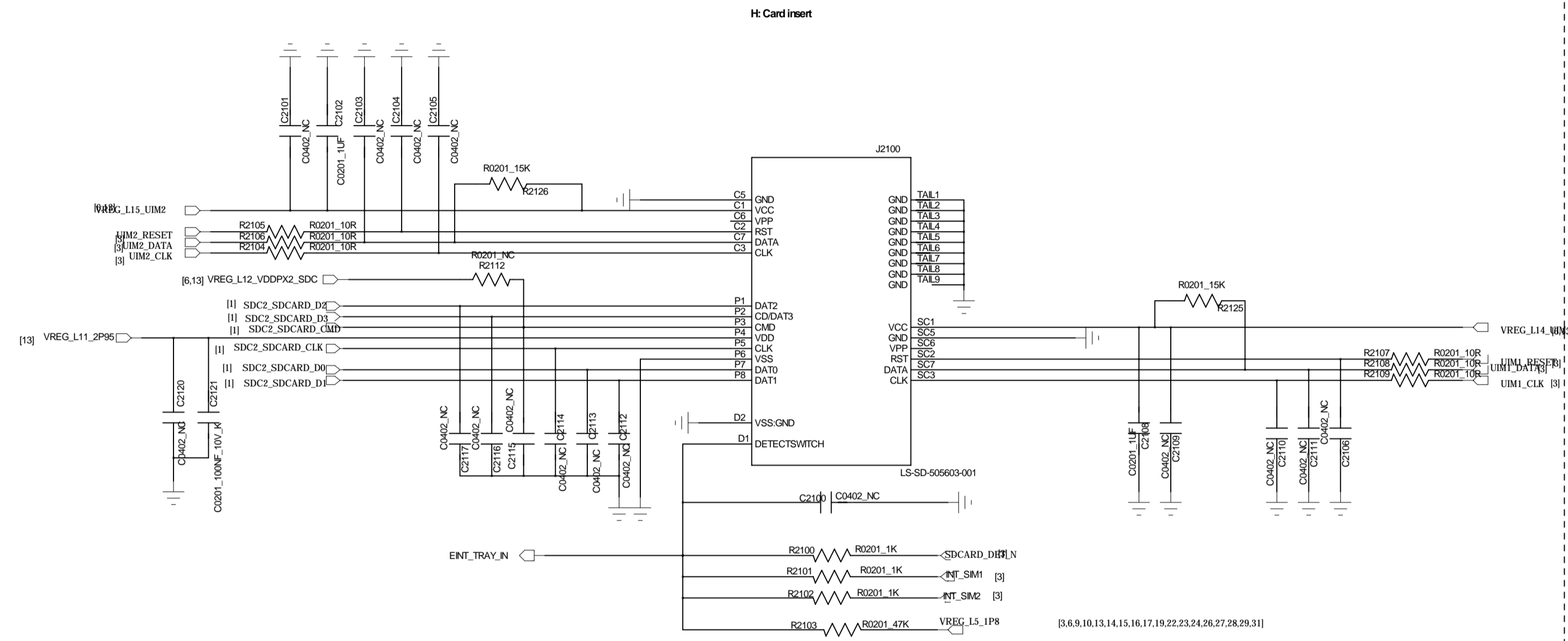


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Audio Interface

Inside: Nano SIM1/outside: T_Flash & Nano SIM2

SIM1 -> Inside
 SIM2 -> Outside
 SW2/CD
 L: Card remove
 H: Card insert

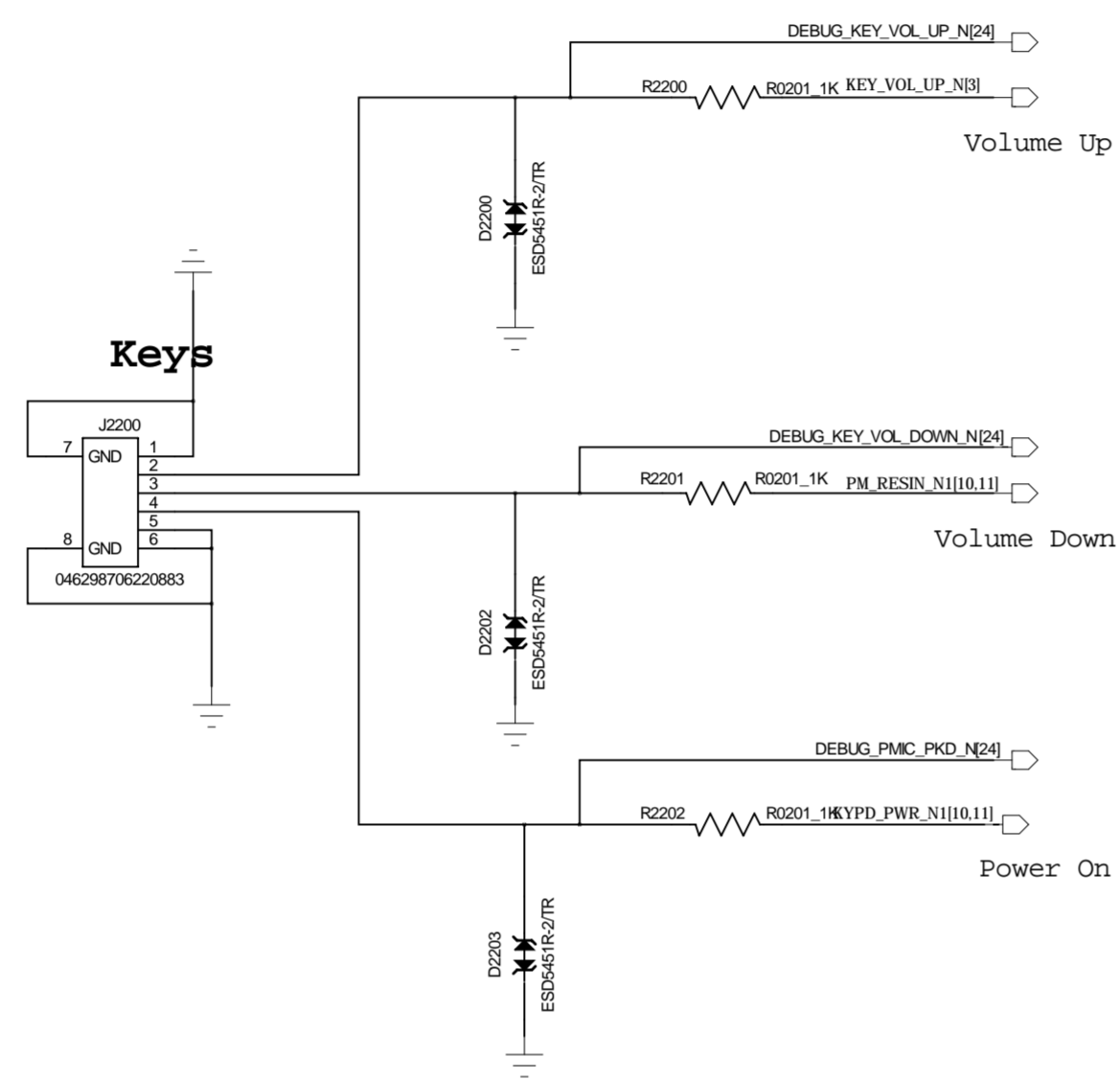


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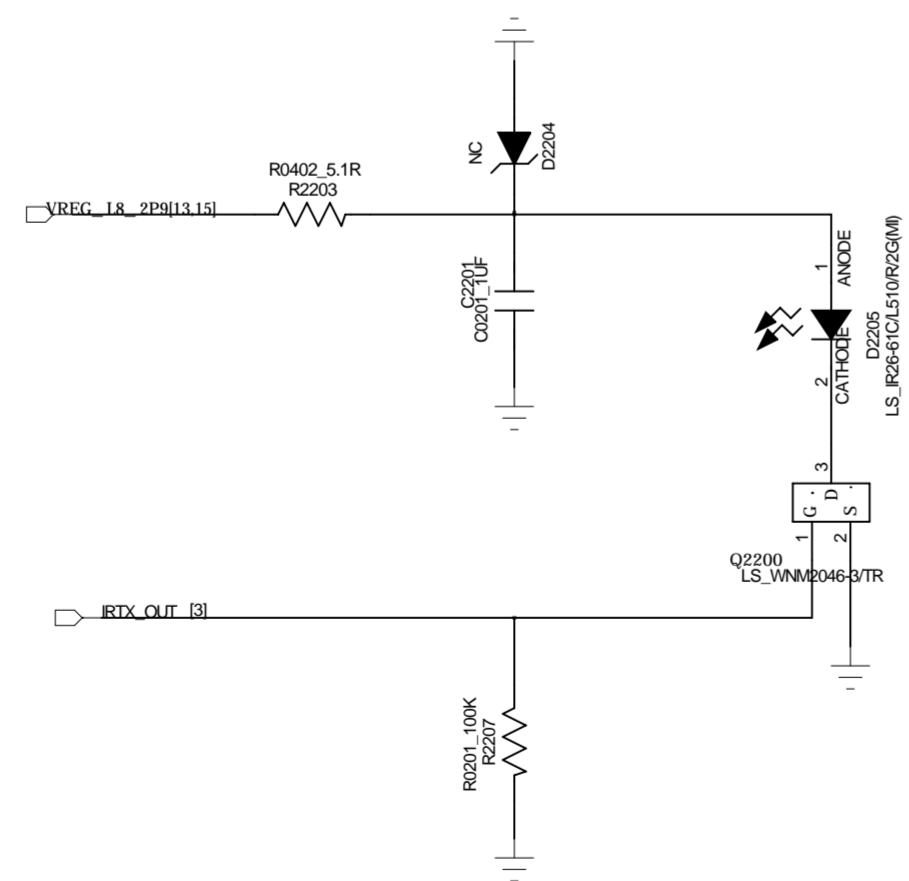
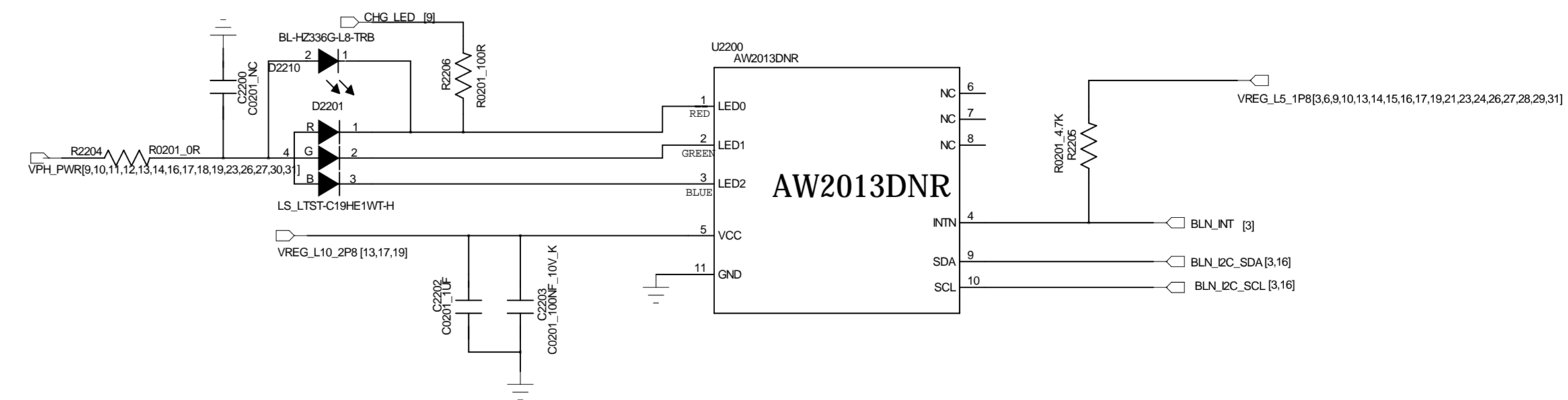
SIM/TF card

QUALCOMM Technologies, Inc.
 3501 La Jolla Village Drive
 San Diego, CA 92121-1714
 U.S.A.

Title		Sheet	
Size	Name	Date	Rev
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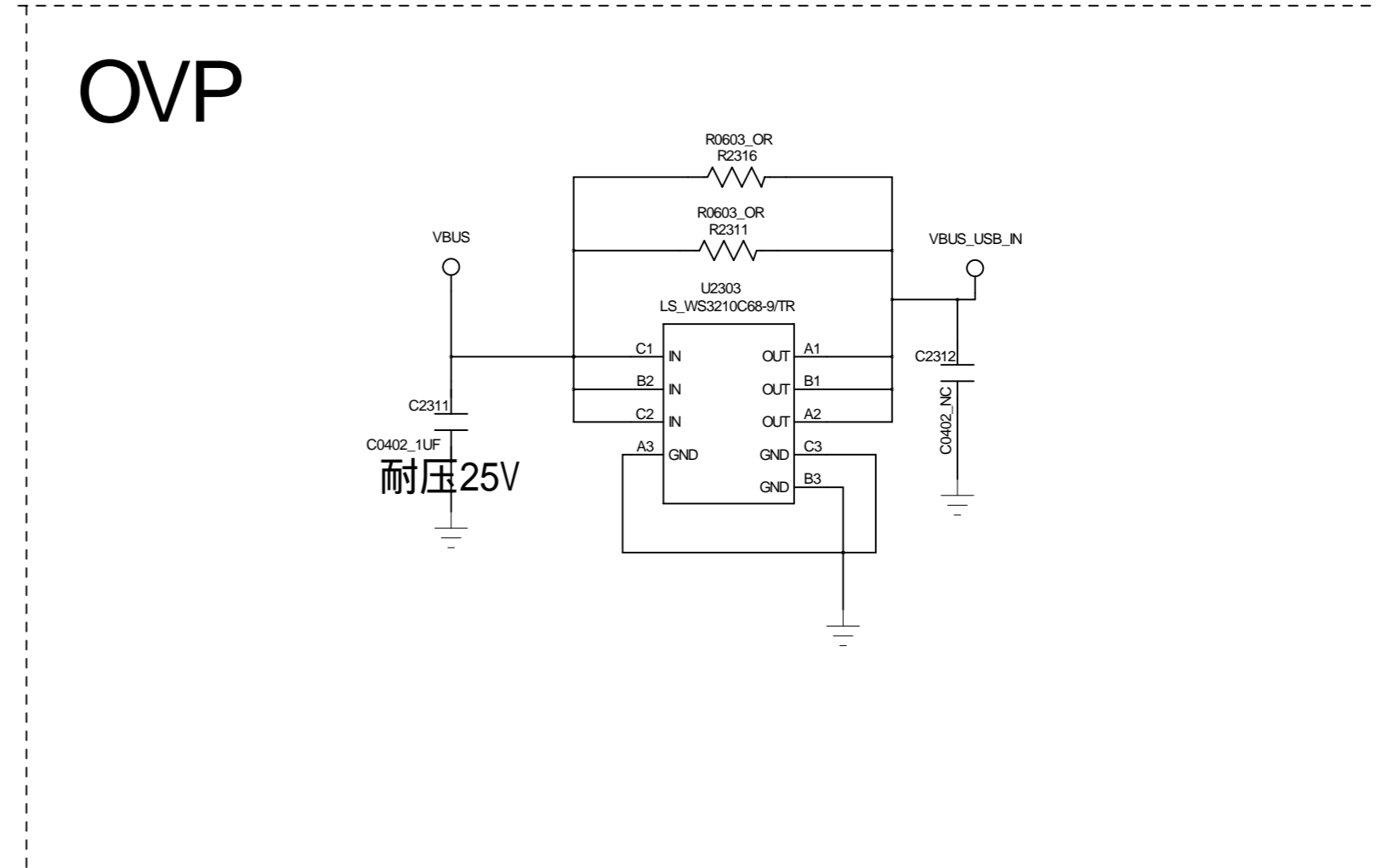
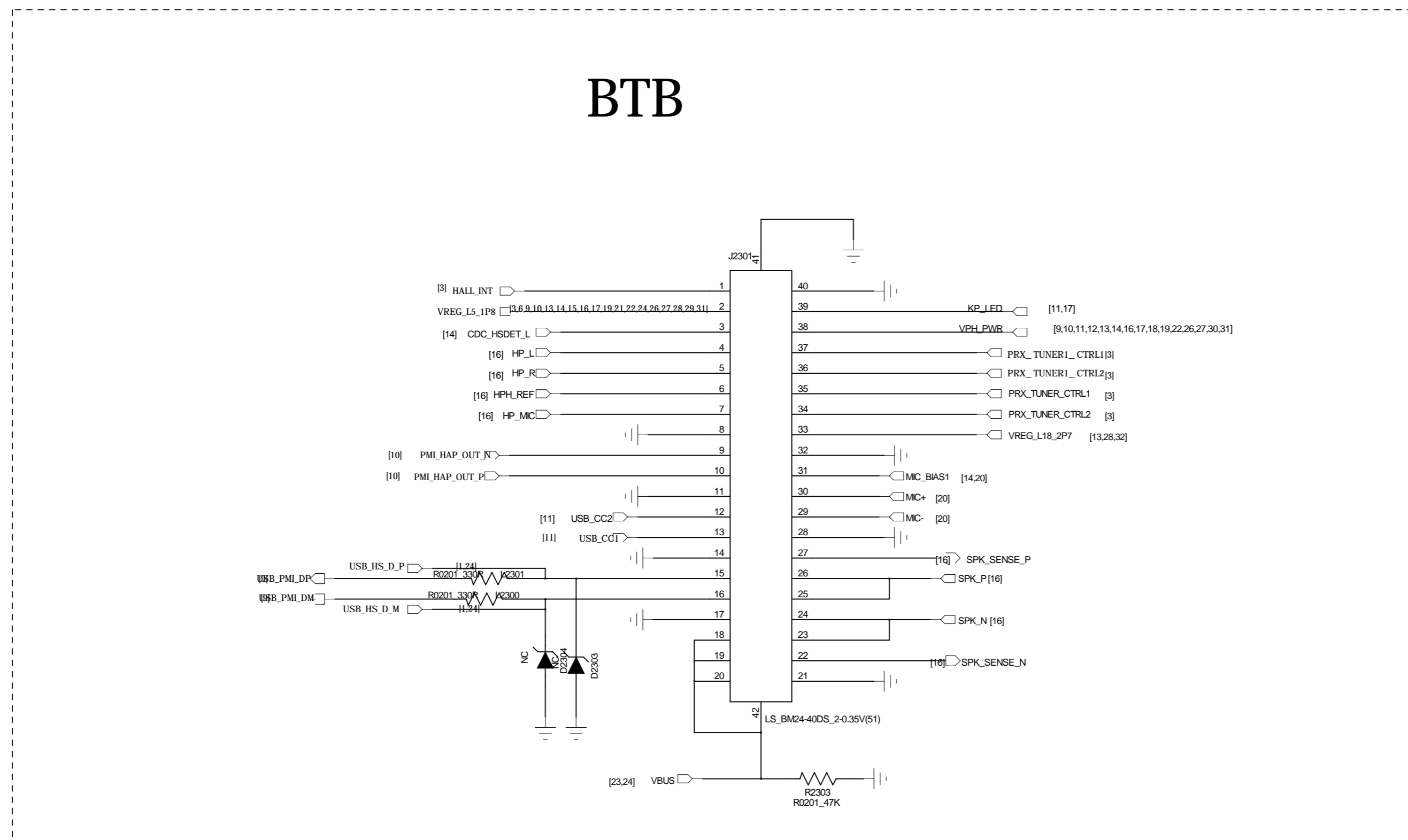
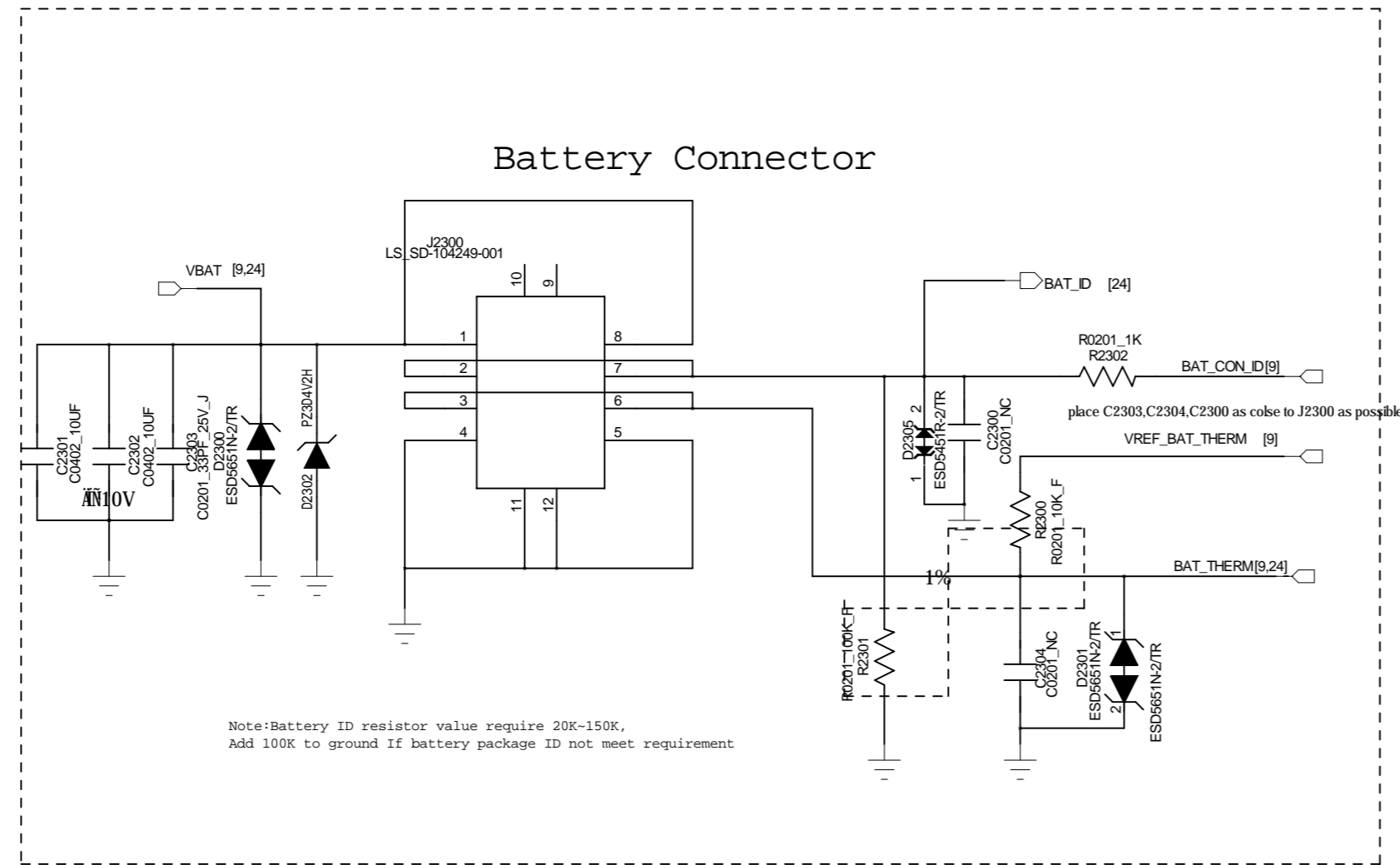


Signal	Description
KPSNS0	Volume Up
PM_RST_N	Volume Down
KYPD_PWR_N	POWER_ON
PM_RST_N + KYPD_PWR_N	Hardware Reset



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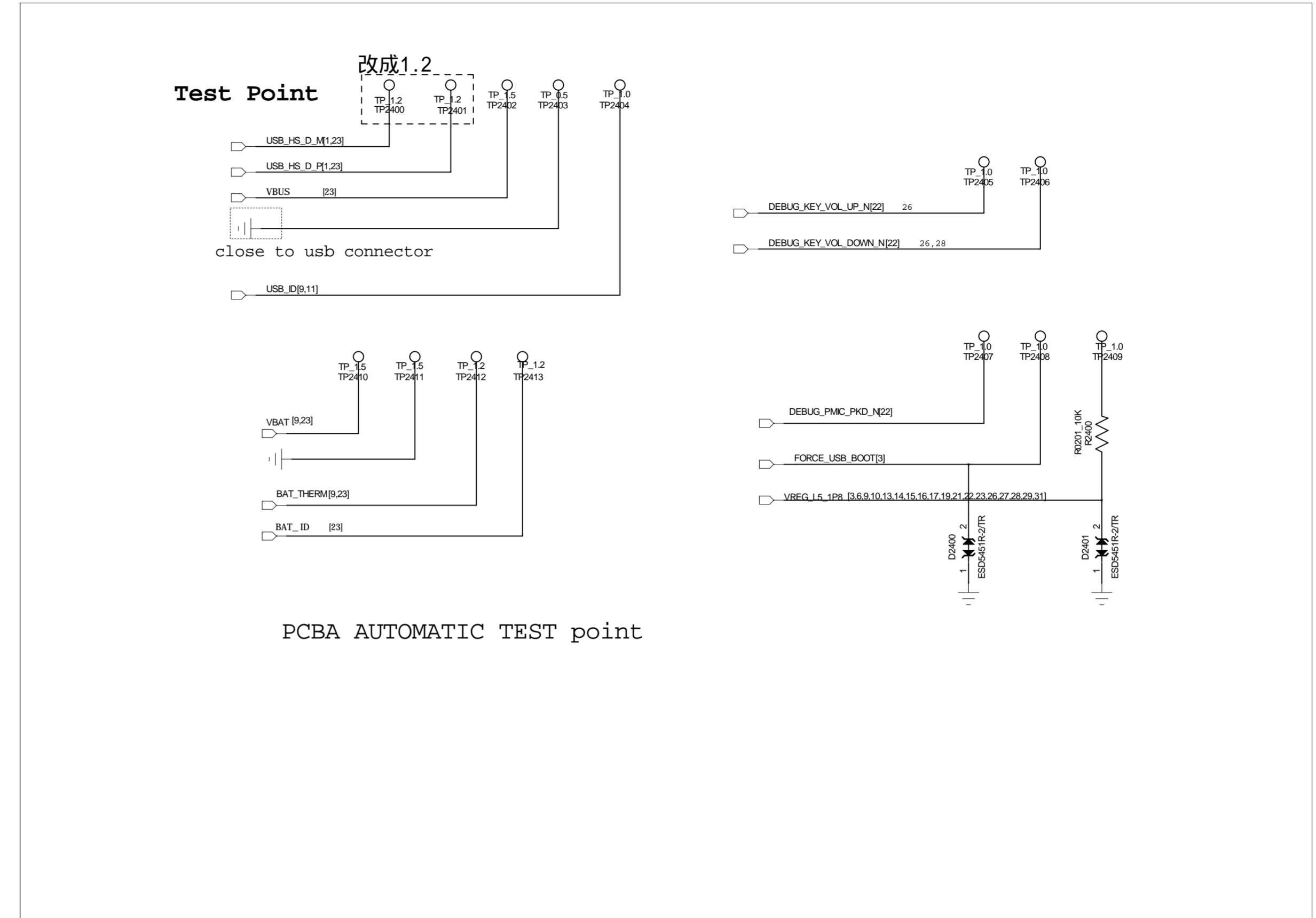
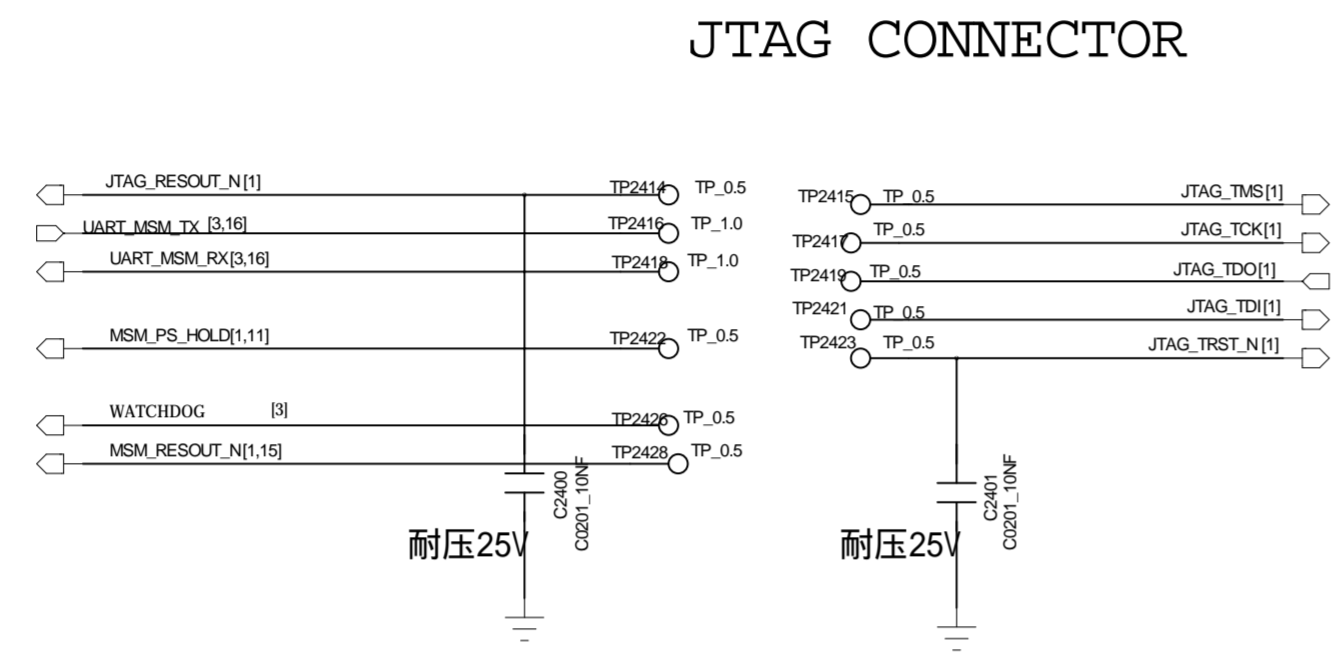
MISC(Keypad/LED/indicator)



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Connector(USB/Sub-board)

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3890 La Jolla Village Drive San Diego, CA 92121-1714 U.S.A.	
Title	
Sheet	
Size	Name
Date:	Sheet of



F101 FIDUCIAL_WITHPASTE F102 FIDUCIAL_WITHPASTE F103 FIDUCIAL_WITHPASTE F104 FIDUCIAL_WITHPASTE

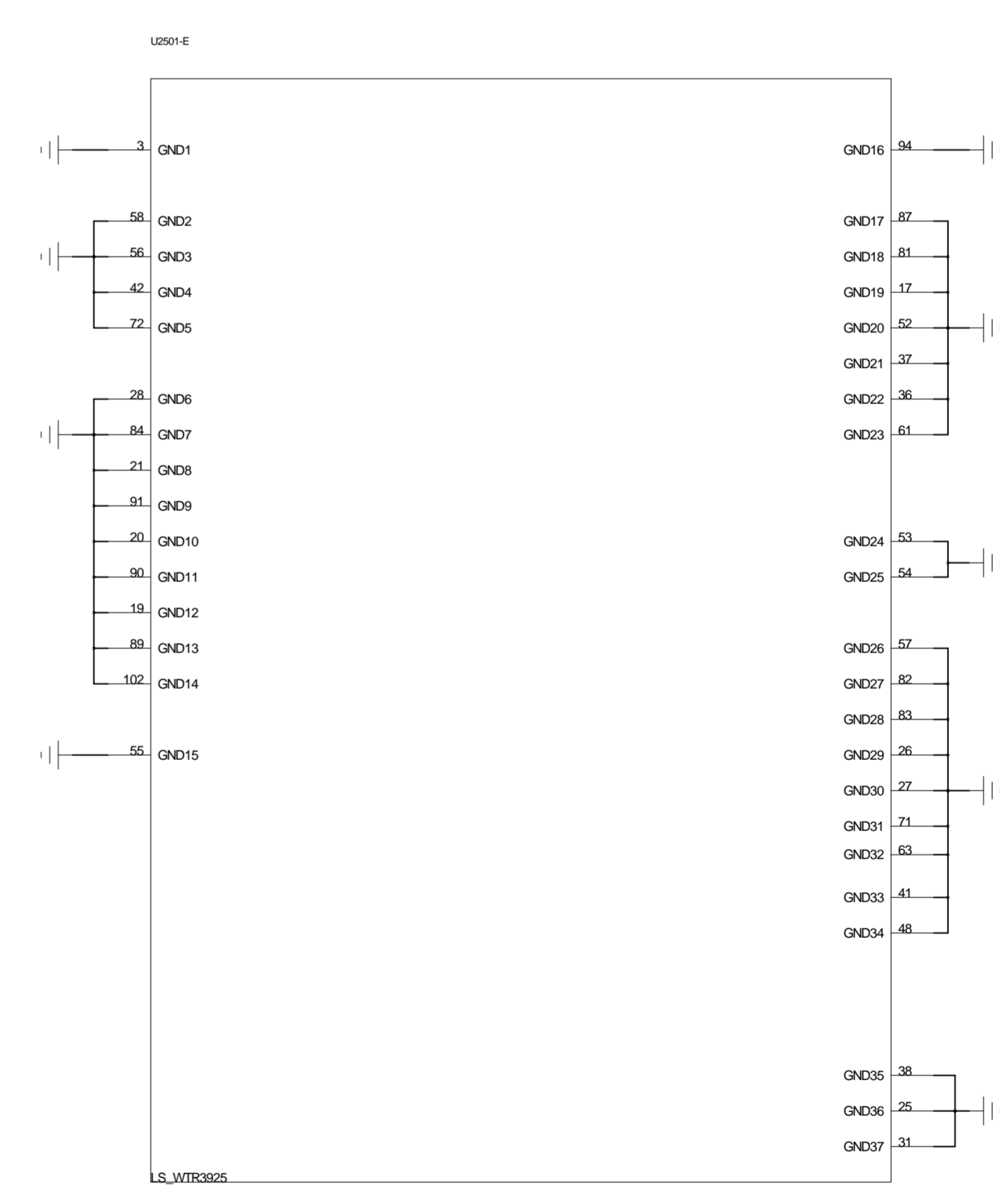
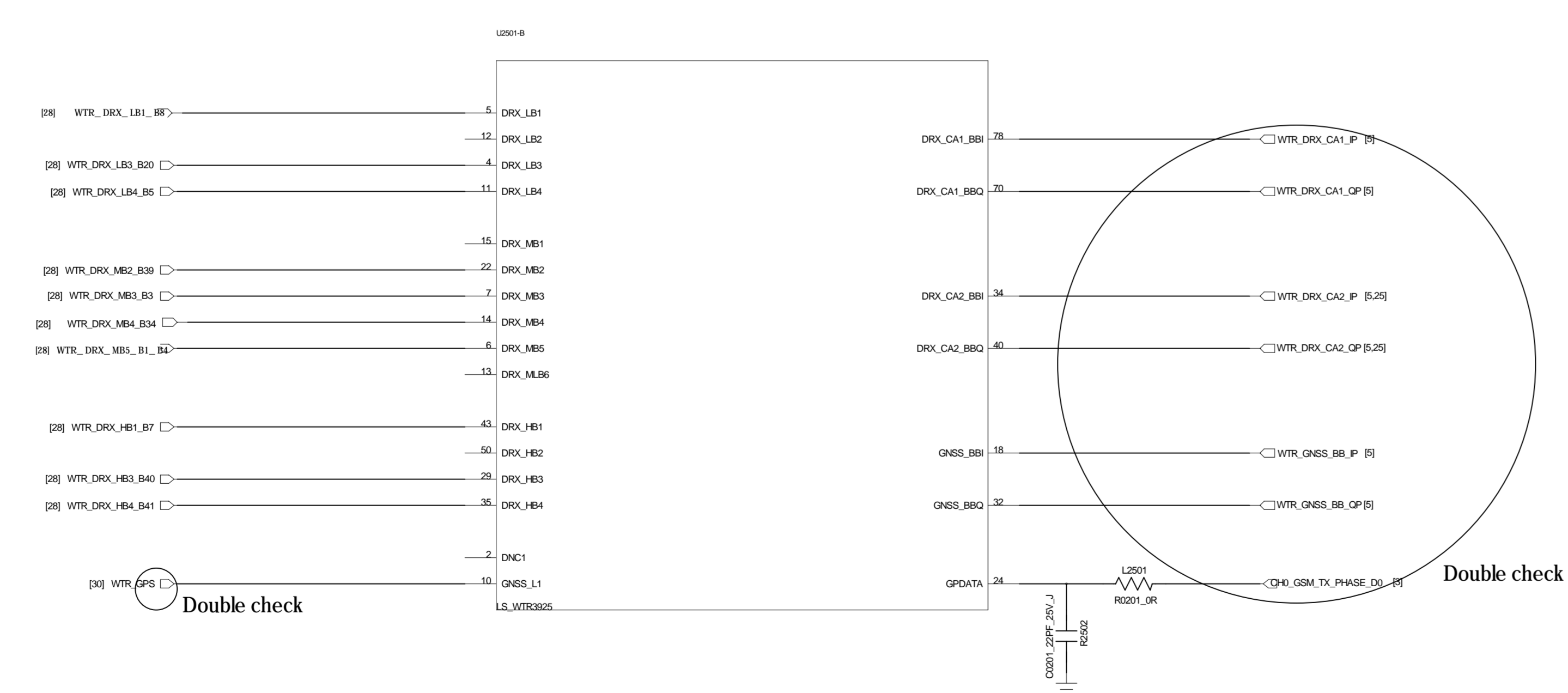
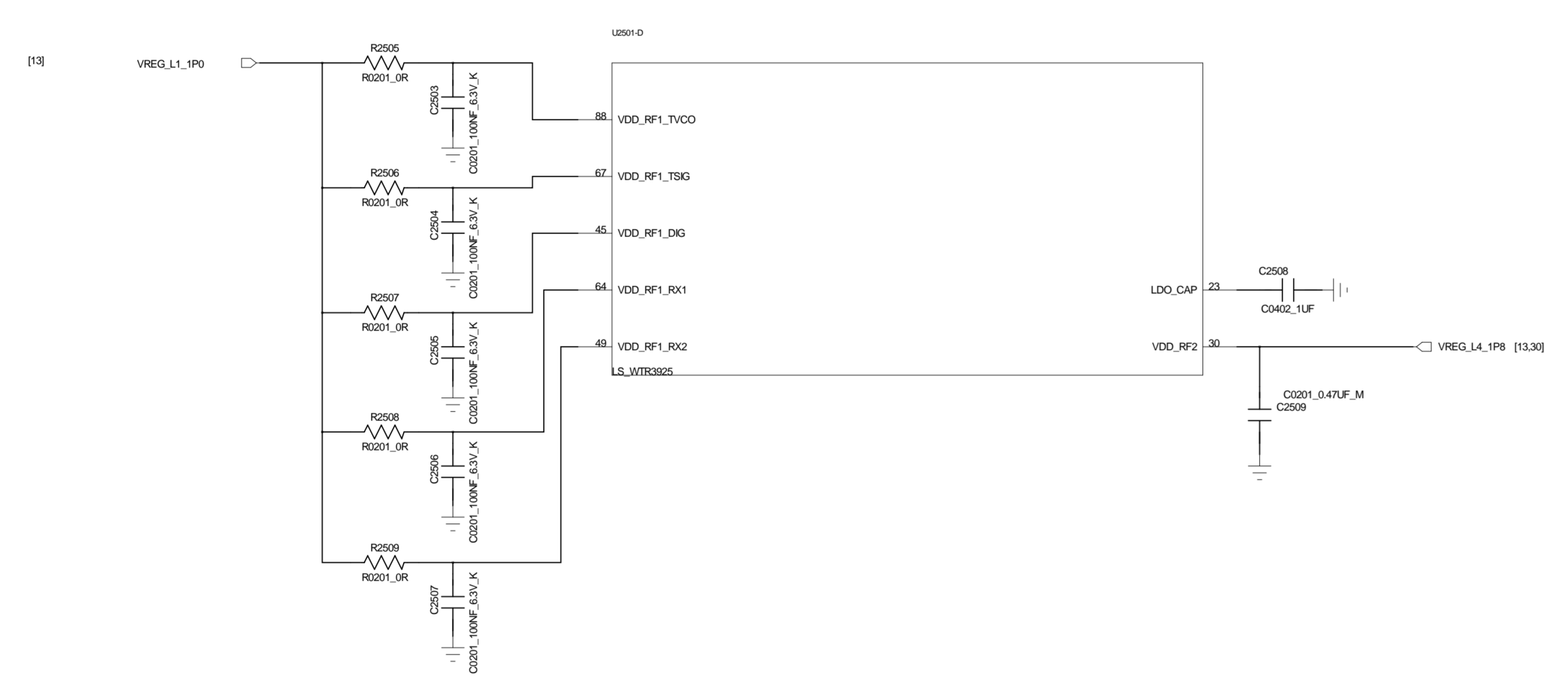
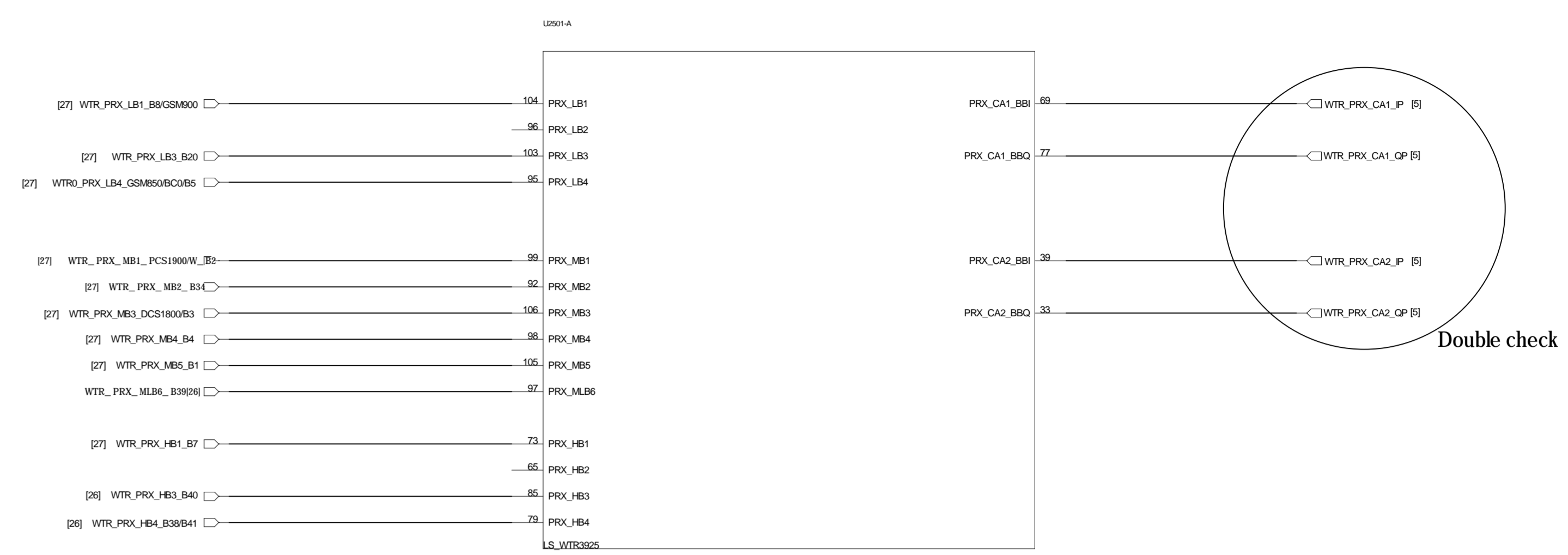
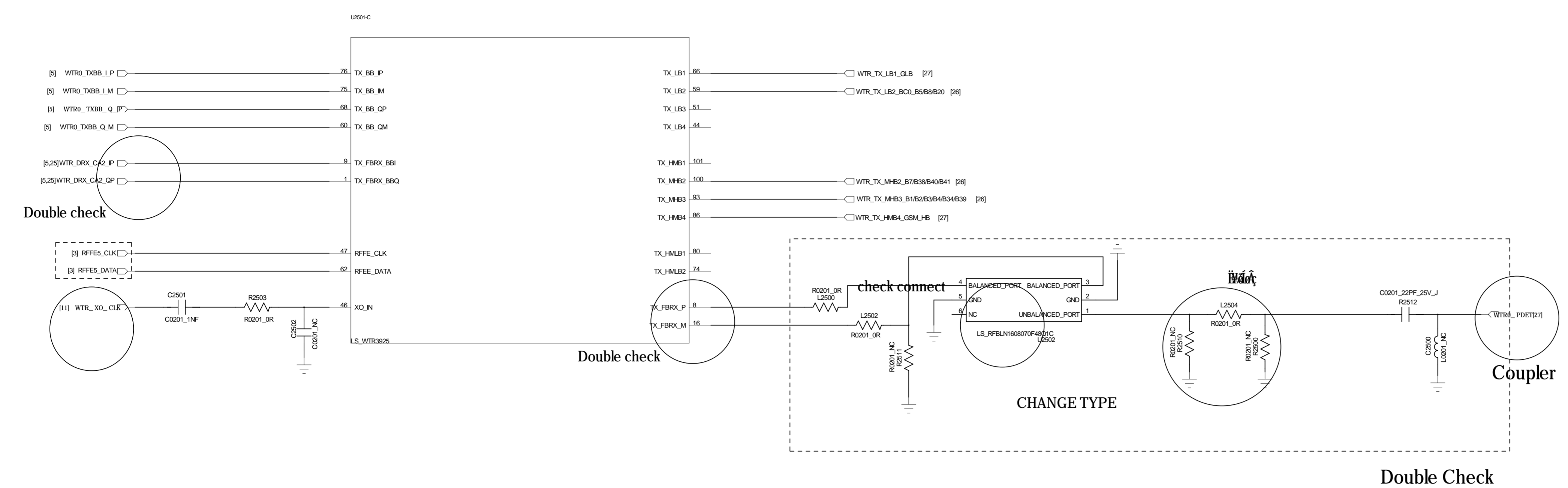


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TP/GND/Shielding

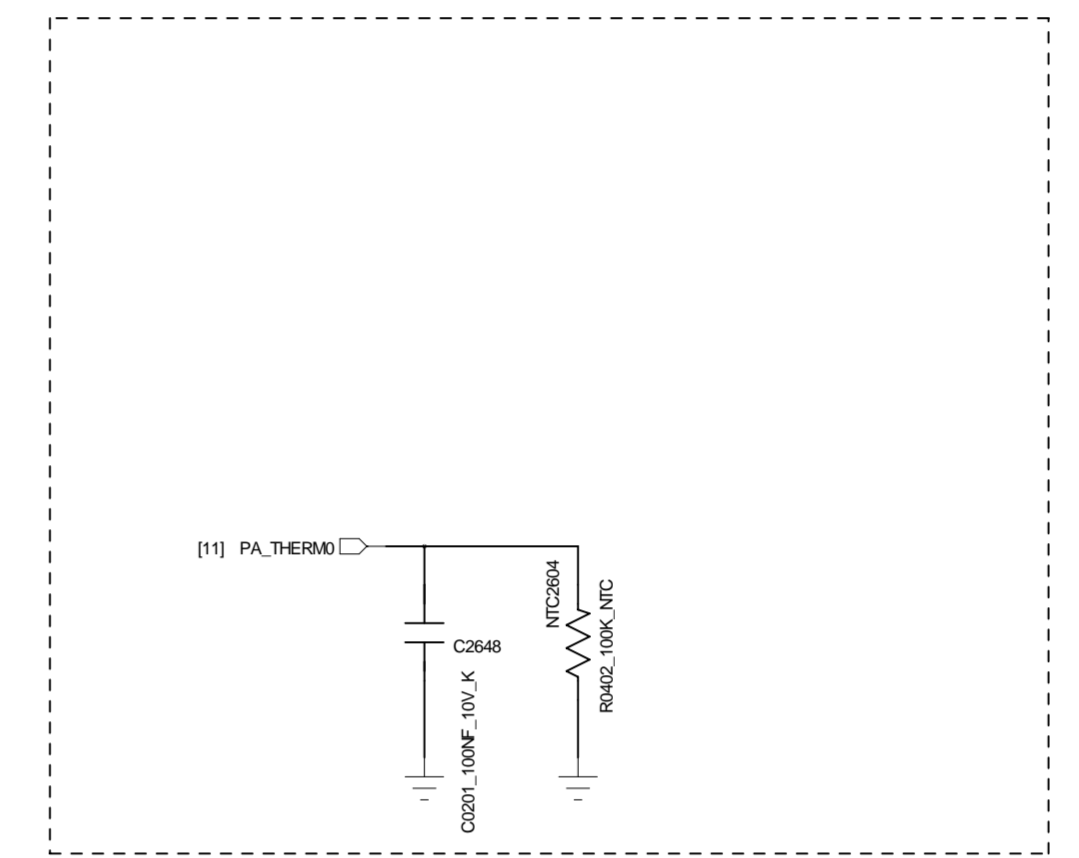
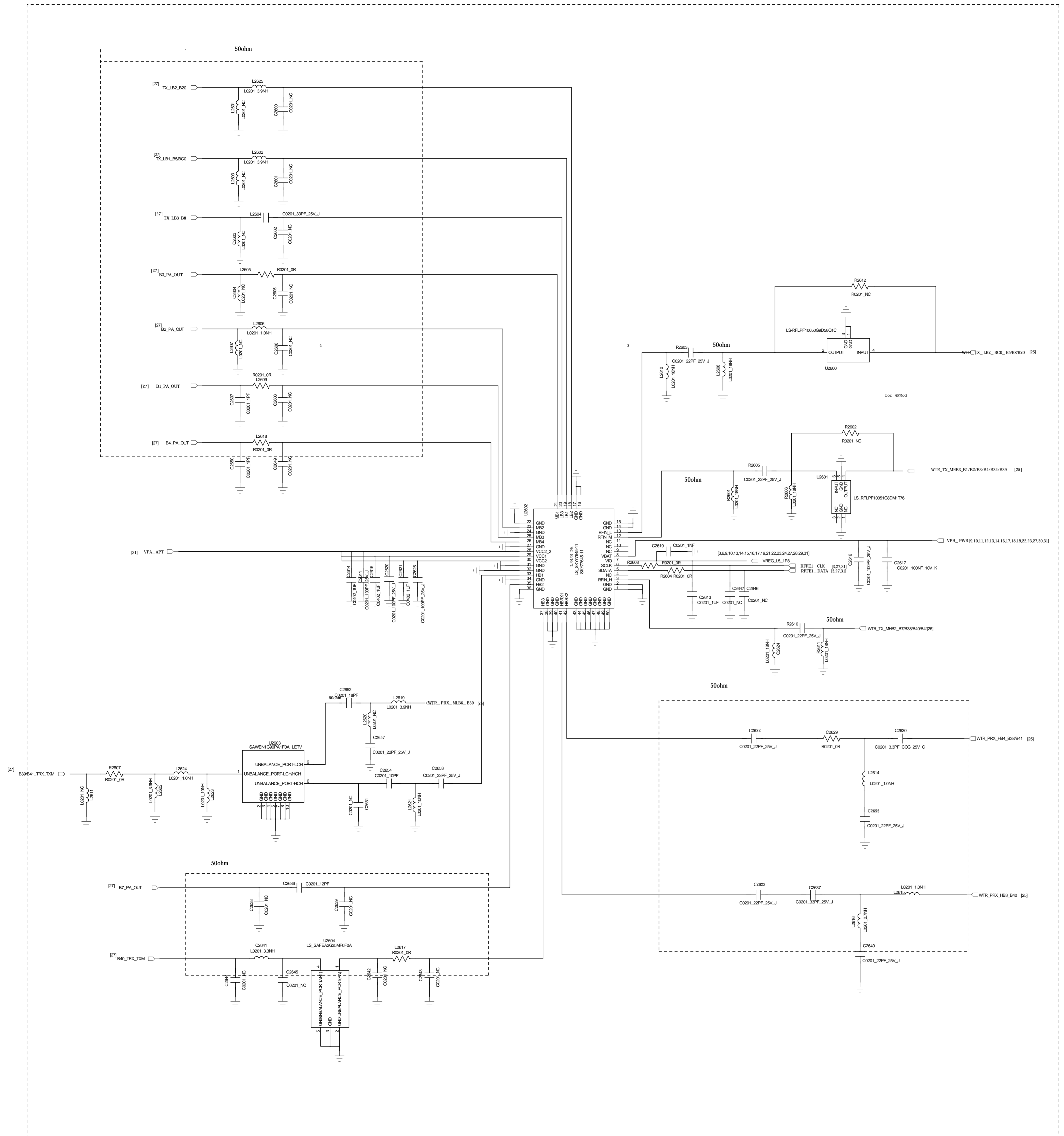
		12860 Innovation Drive San Diego, CA 92121-1714 U.S.A.
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Sheet Size Name	Rev	Date
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REVISION RECORD			
LR	ECONO	APPROVED	DATE



COMPANY: <Company Name>			
TITLE: <Title>			
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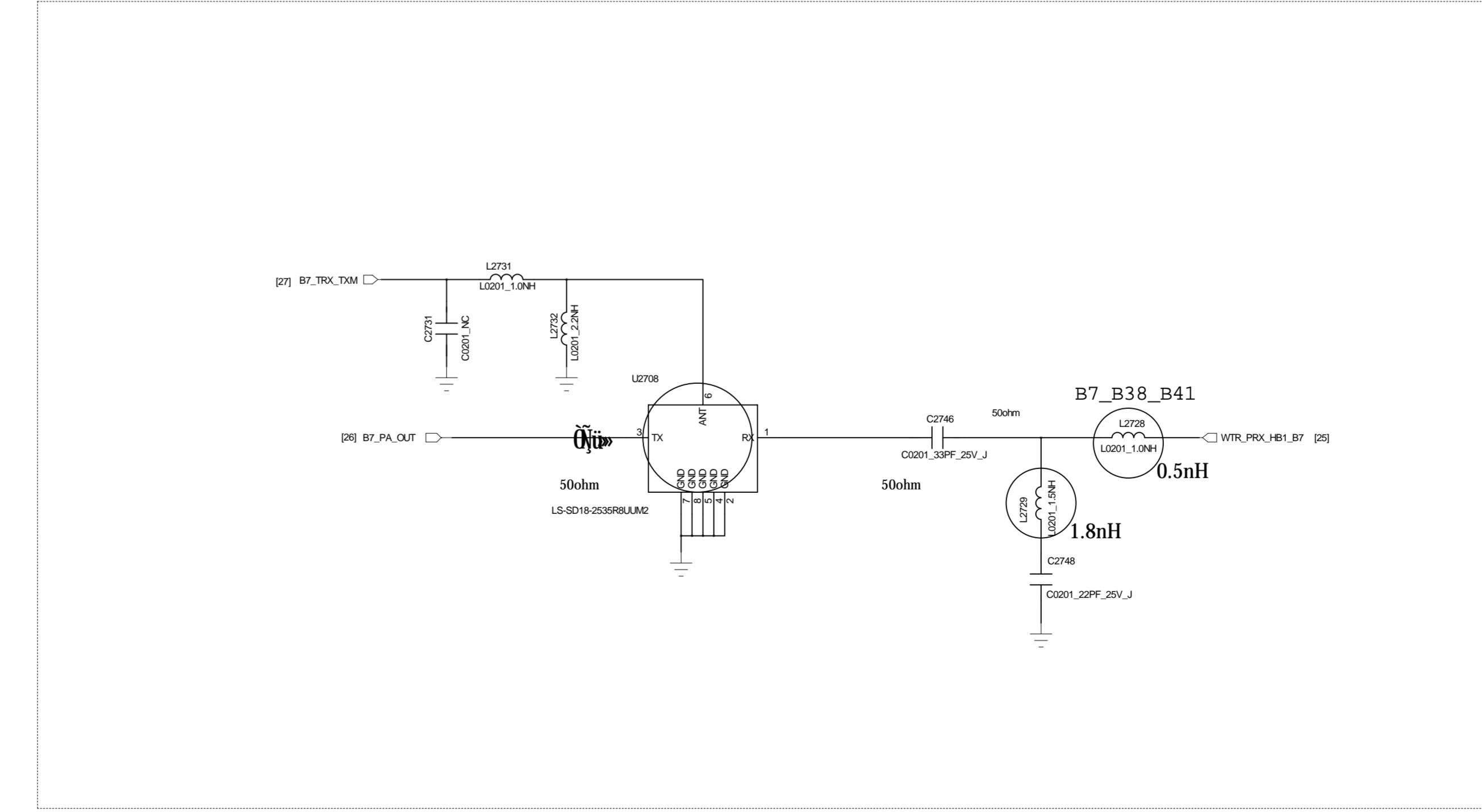
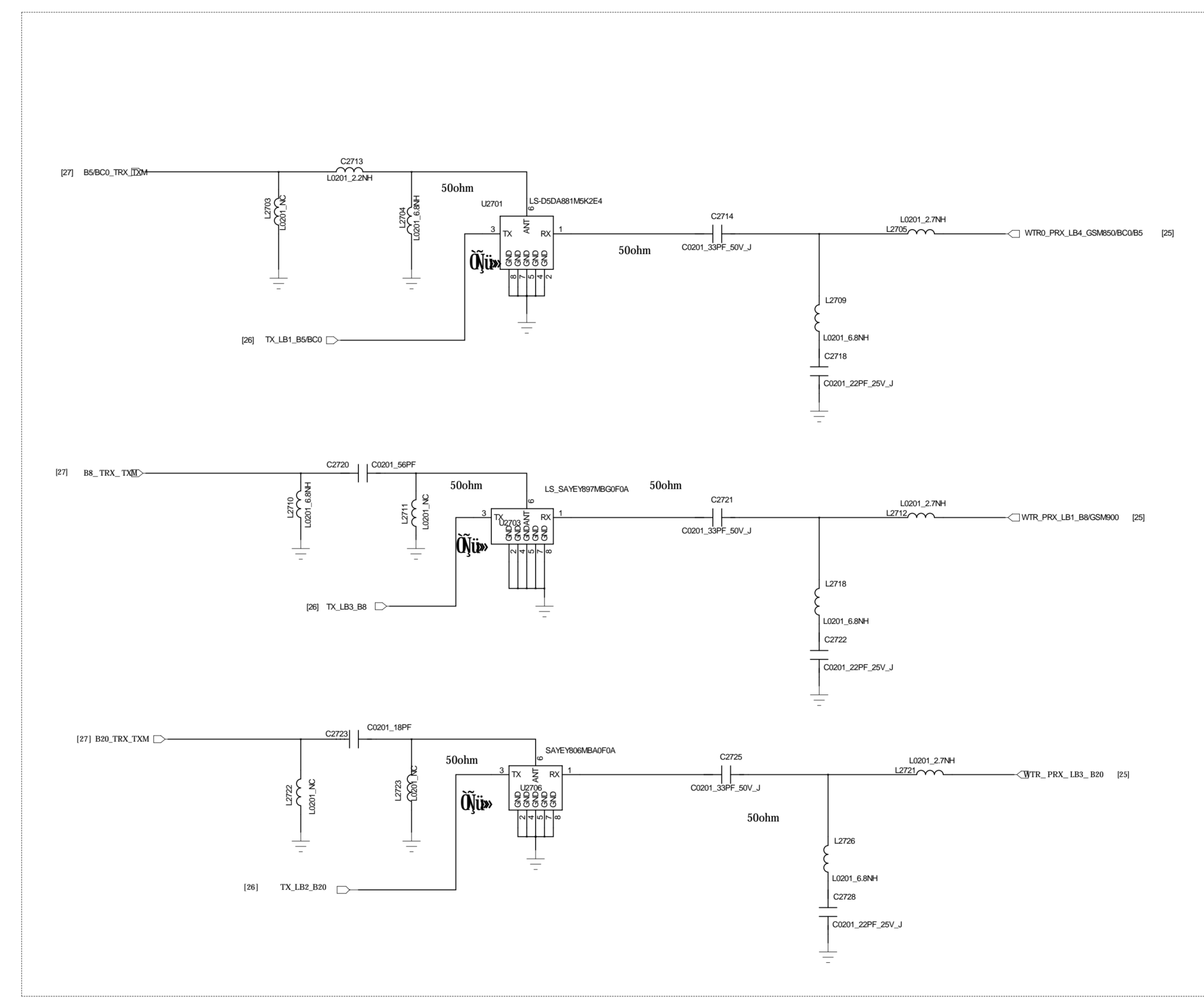
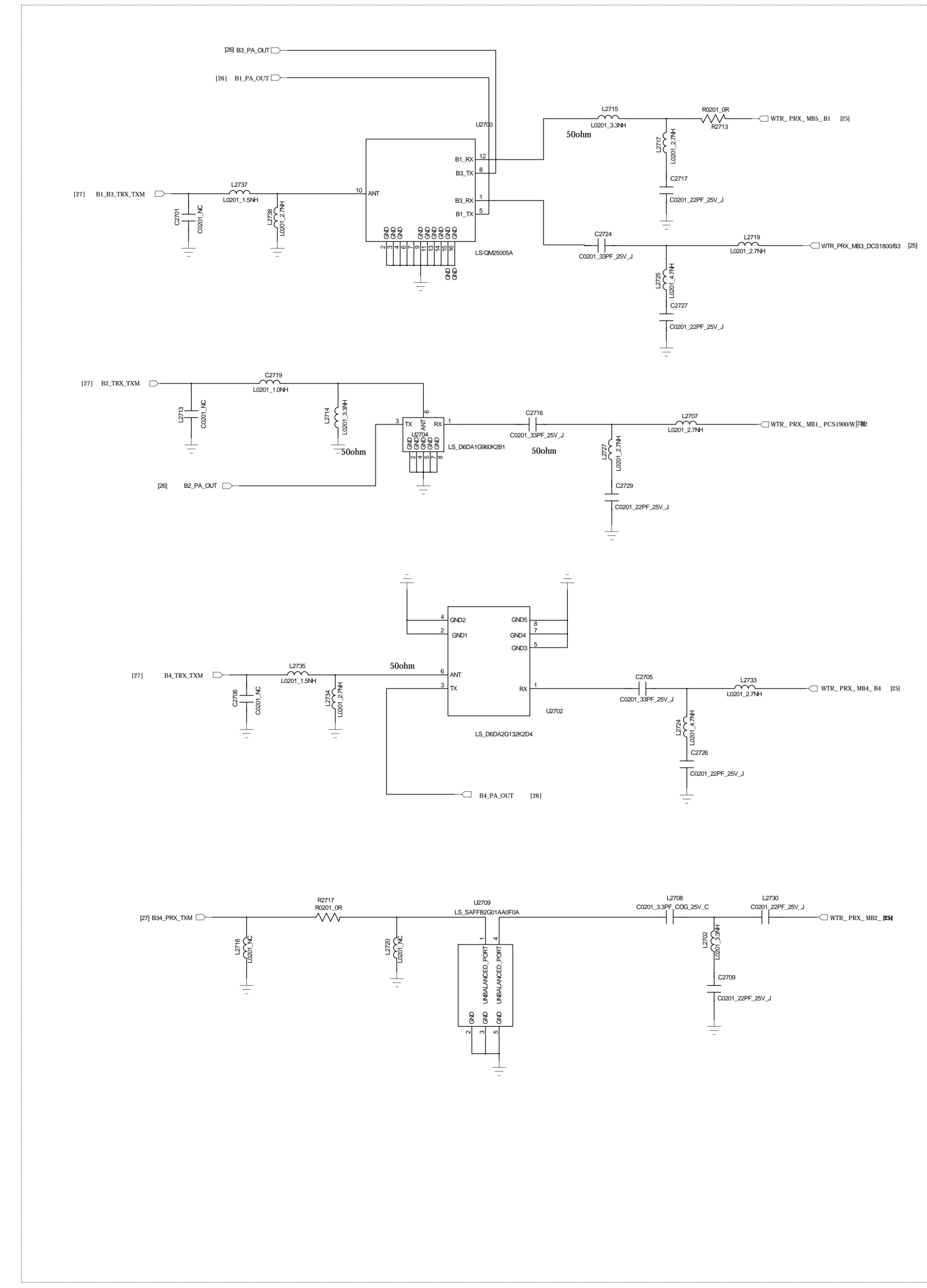
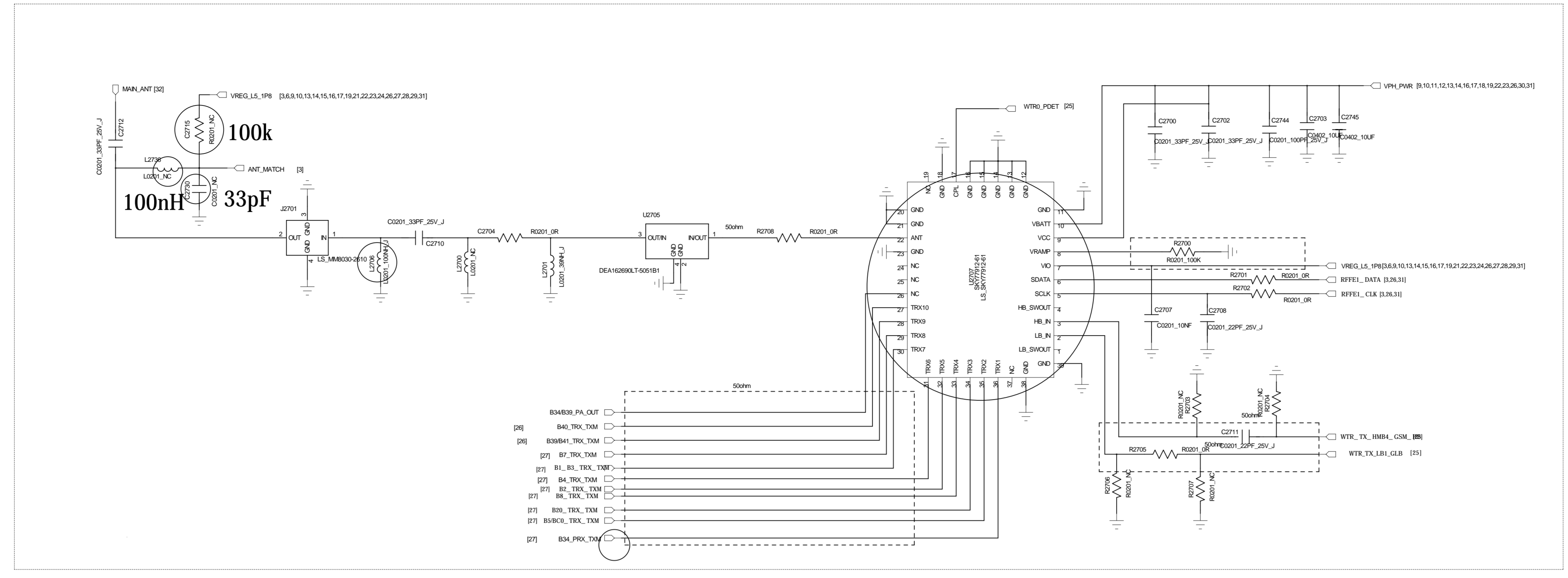
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LR	ECO-NO	APPROVED	DATE



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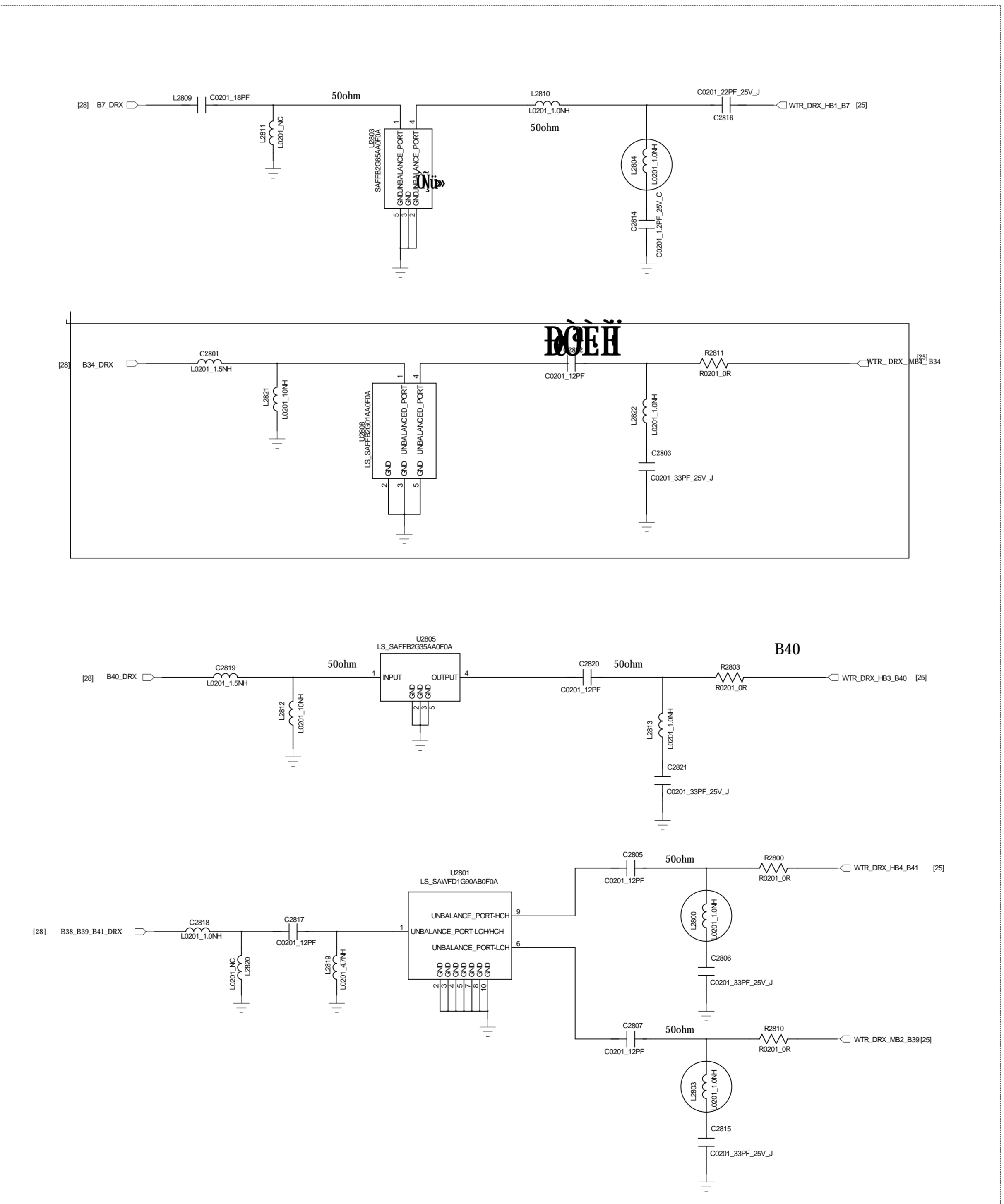
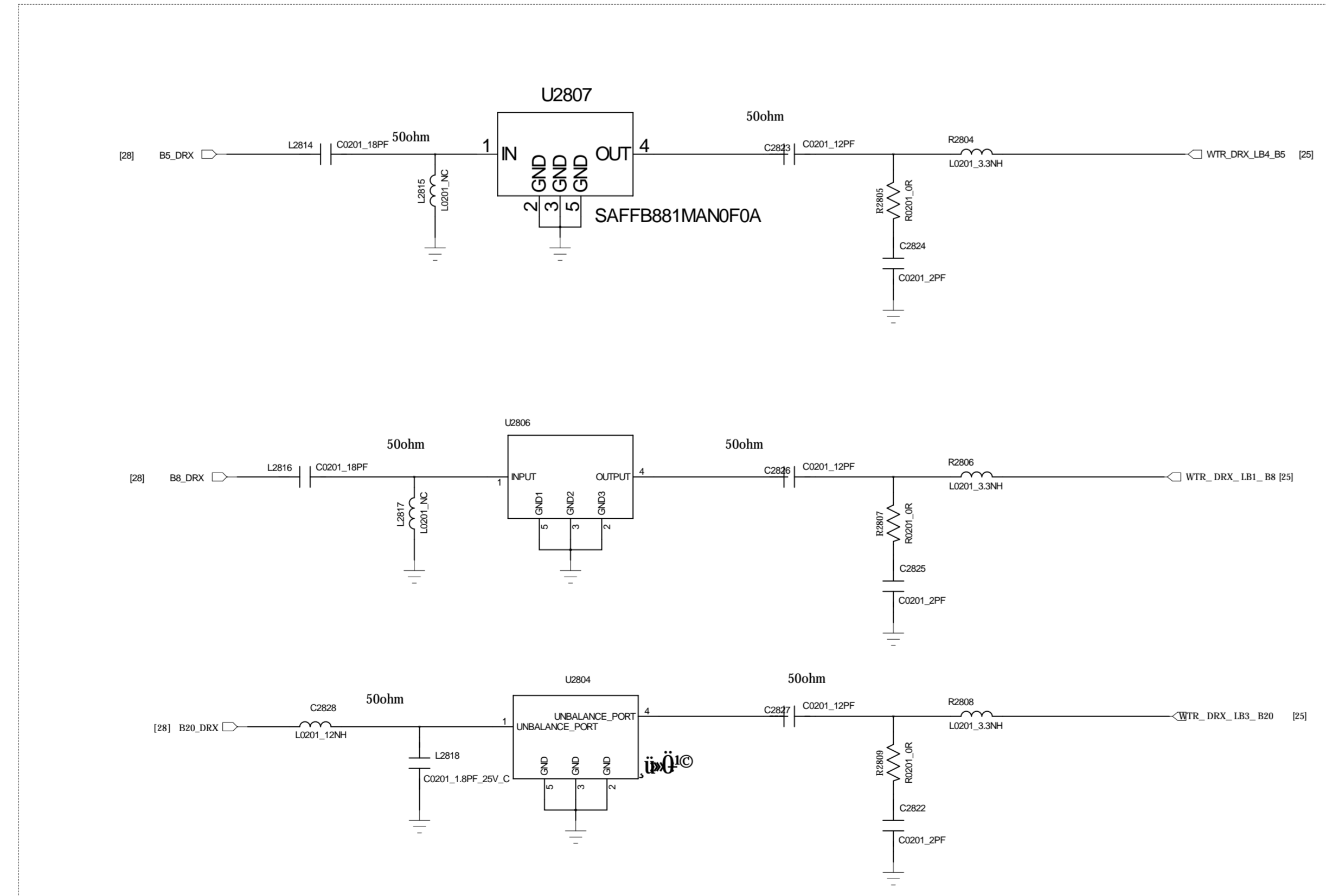
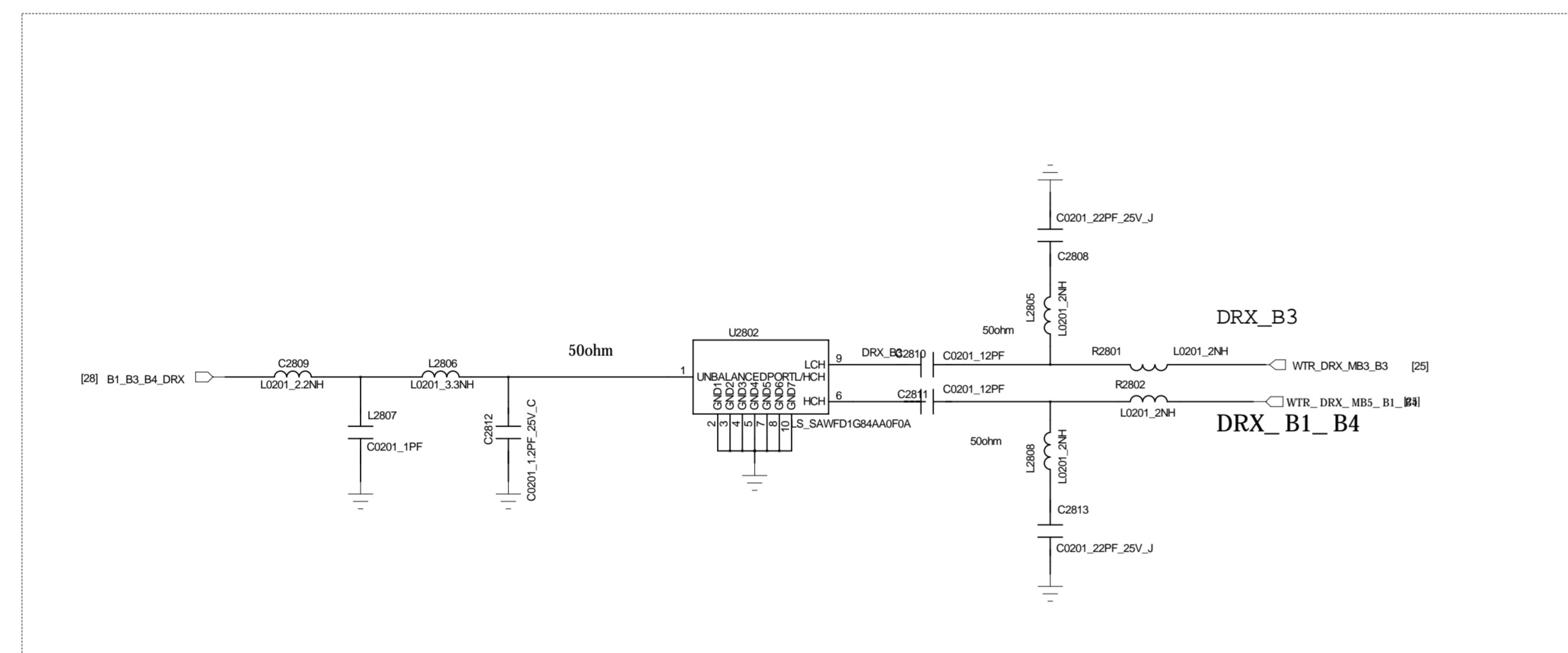
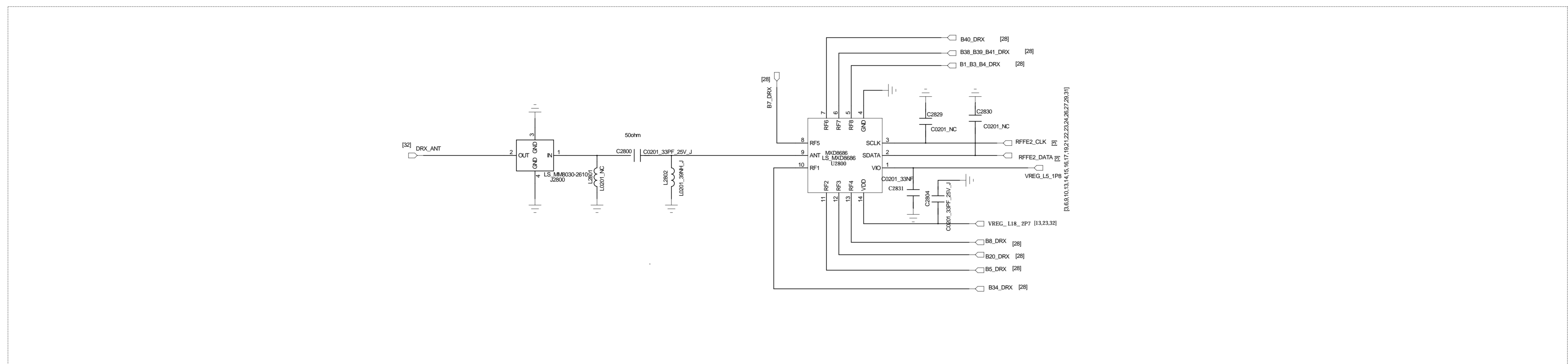


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TITLE: <Title>

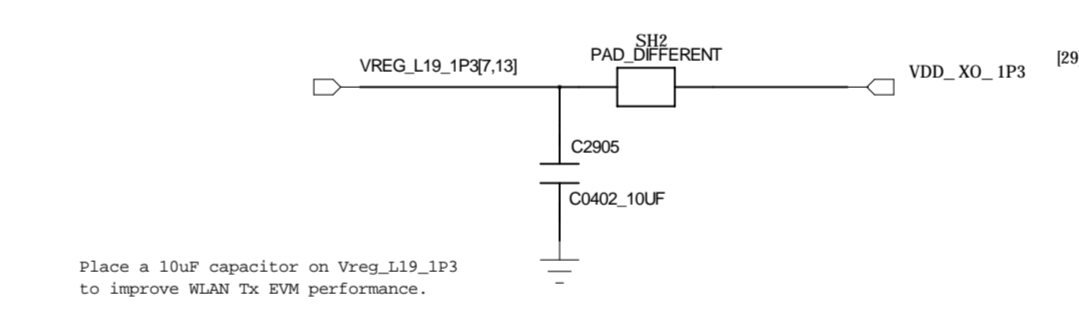
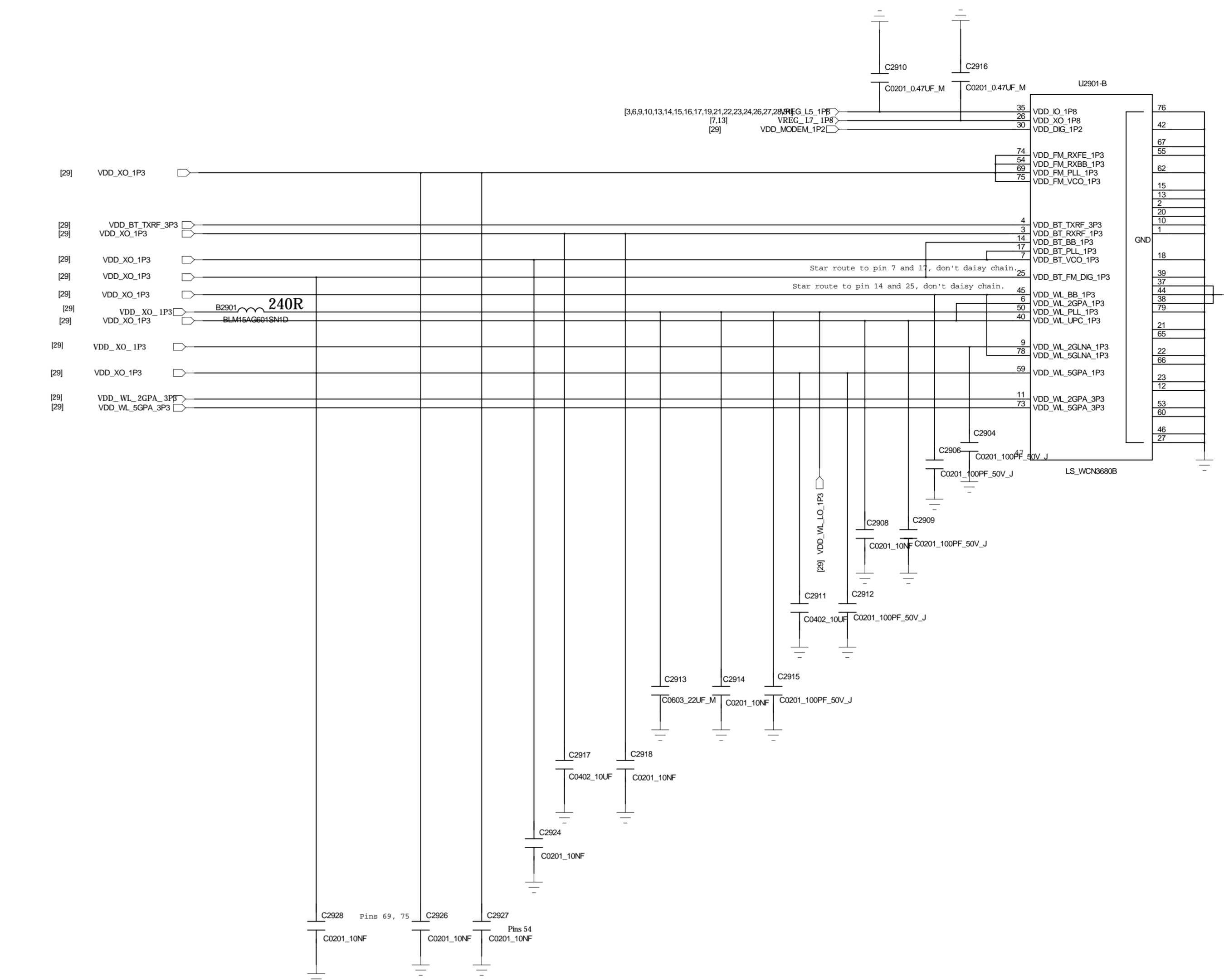
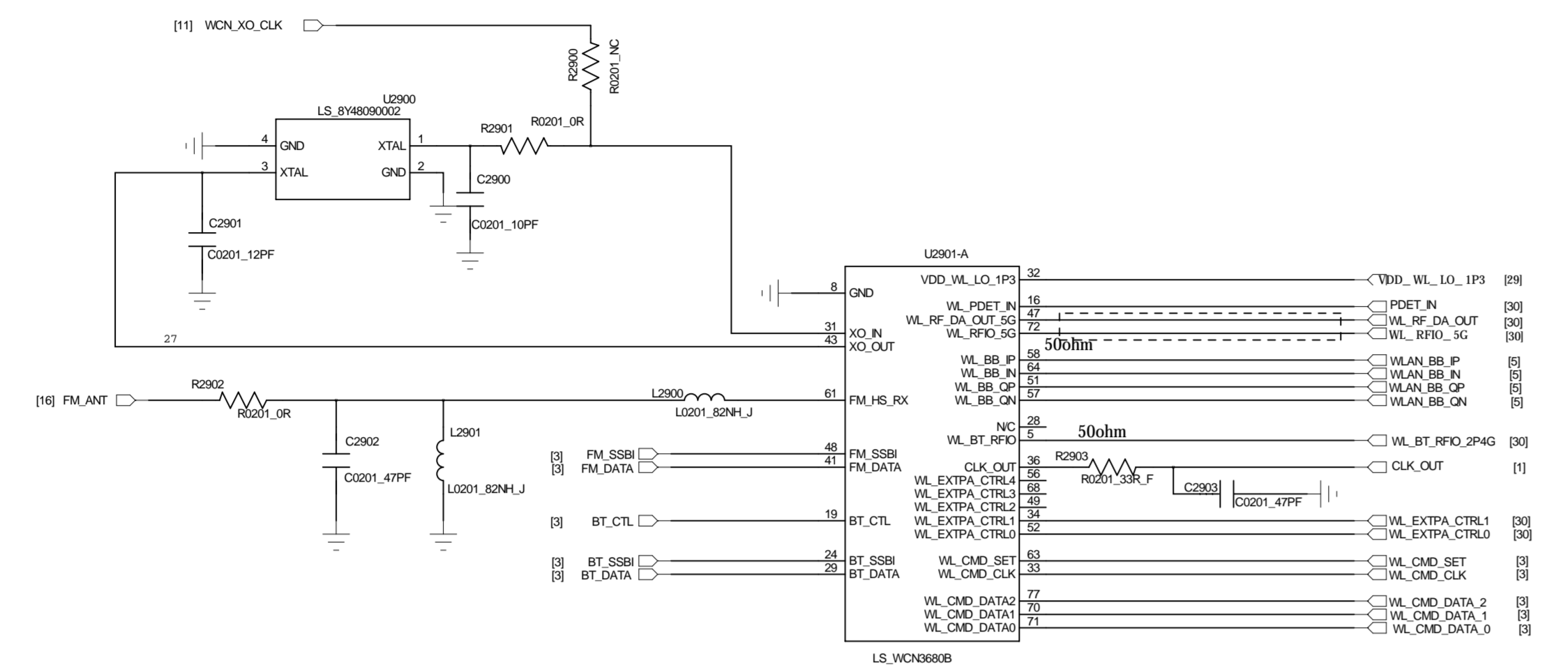
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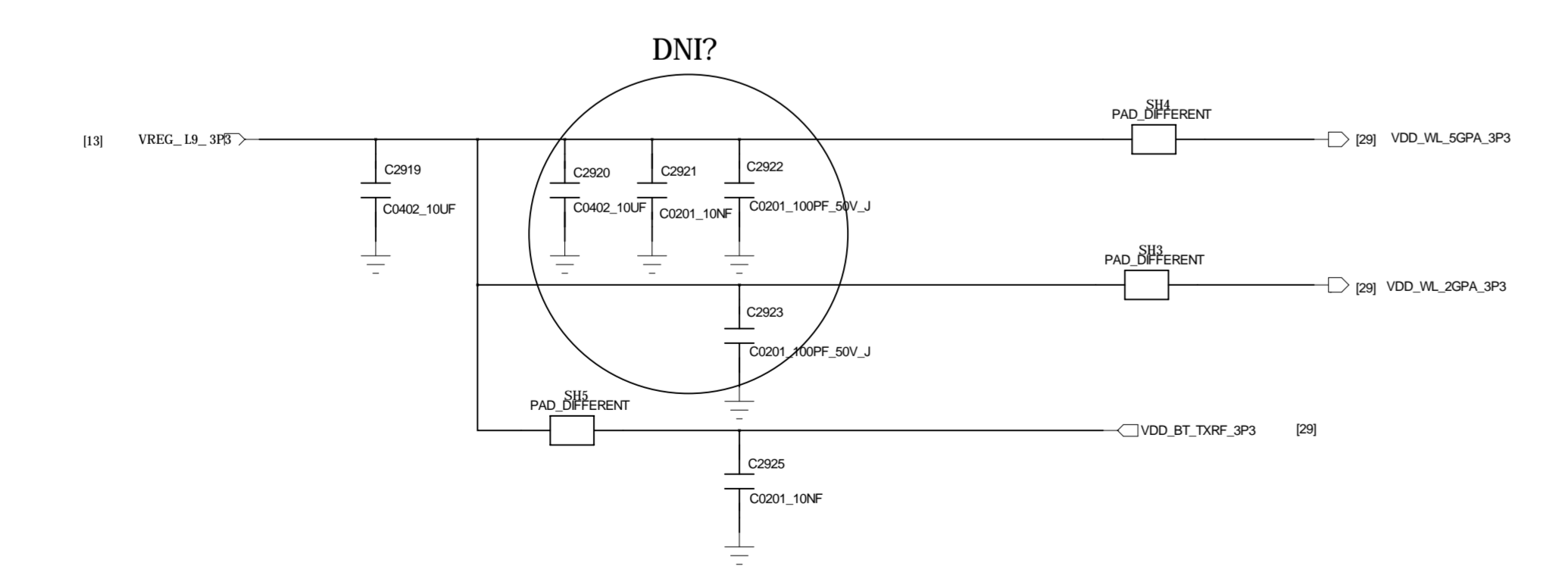


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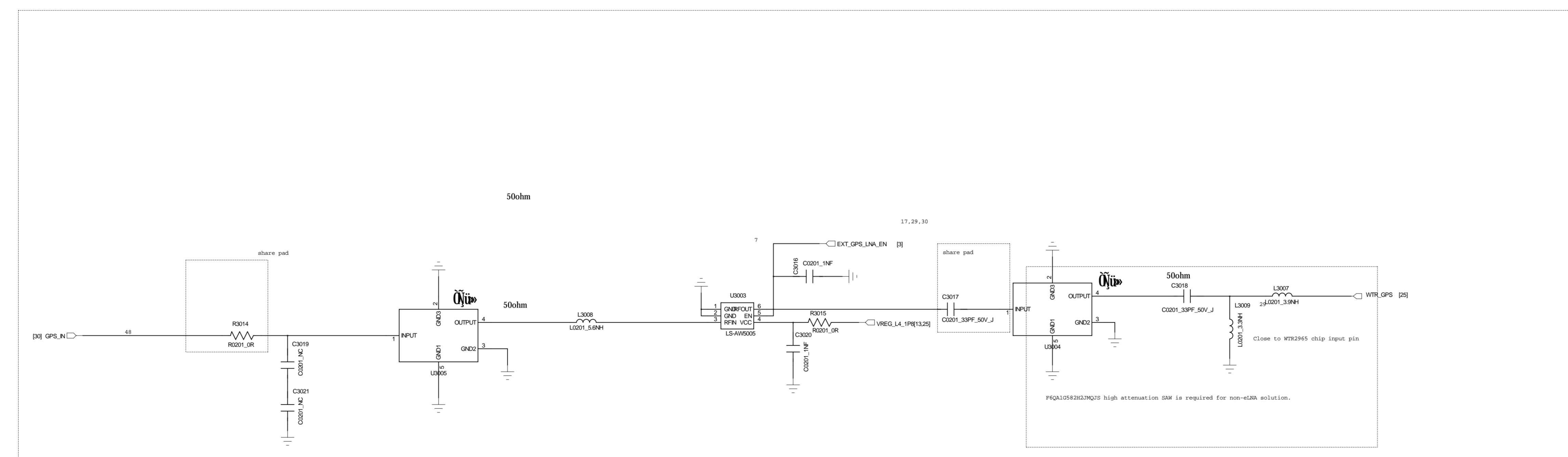
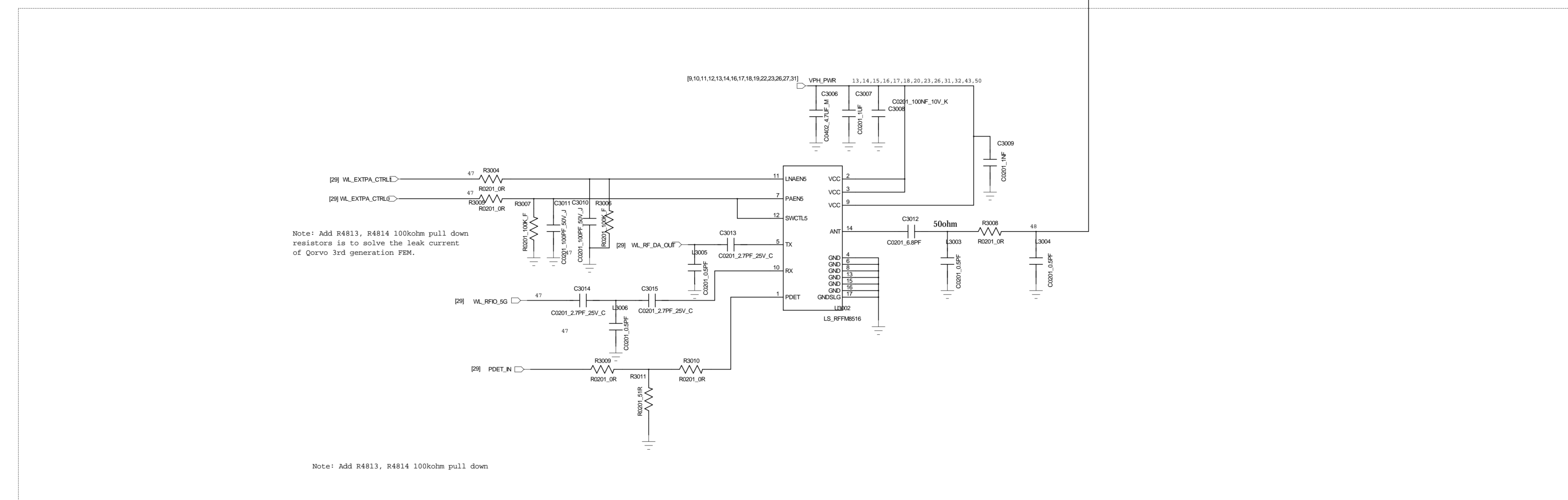
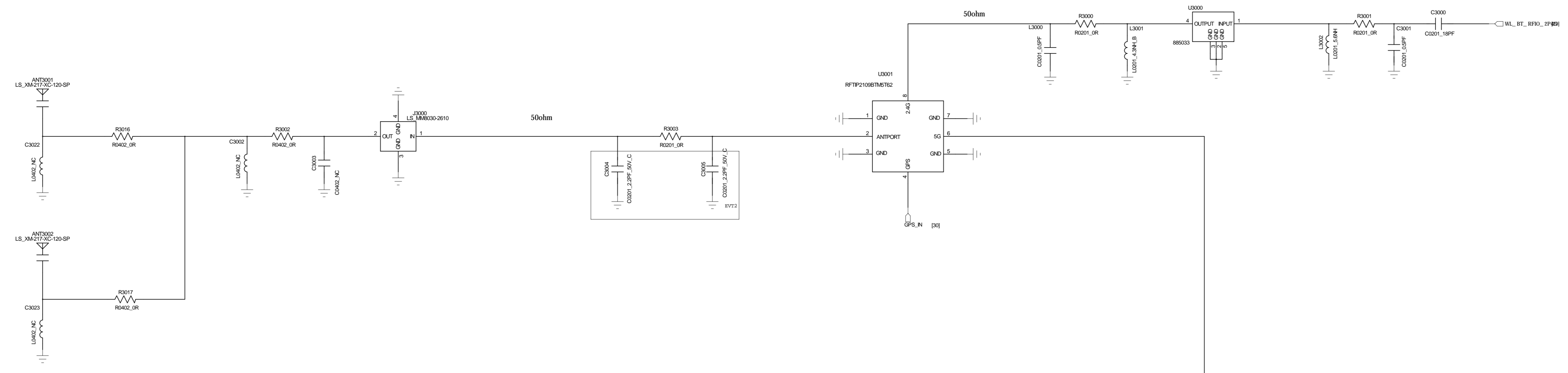
Place a 22R resistor on VREG_VDD to improve ALU to RAM performance.



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DRAWN: <Drawn By>		DATE: <Drawn Date>		COMPANY: <Company Name>	
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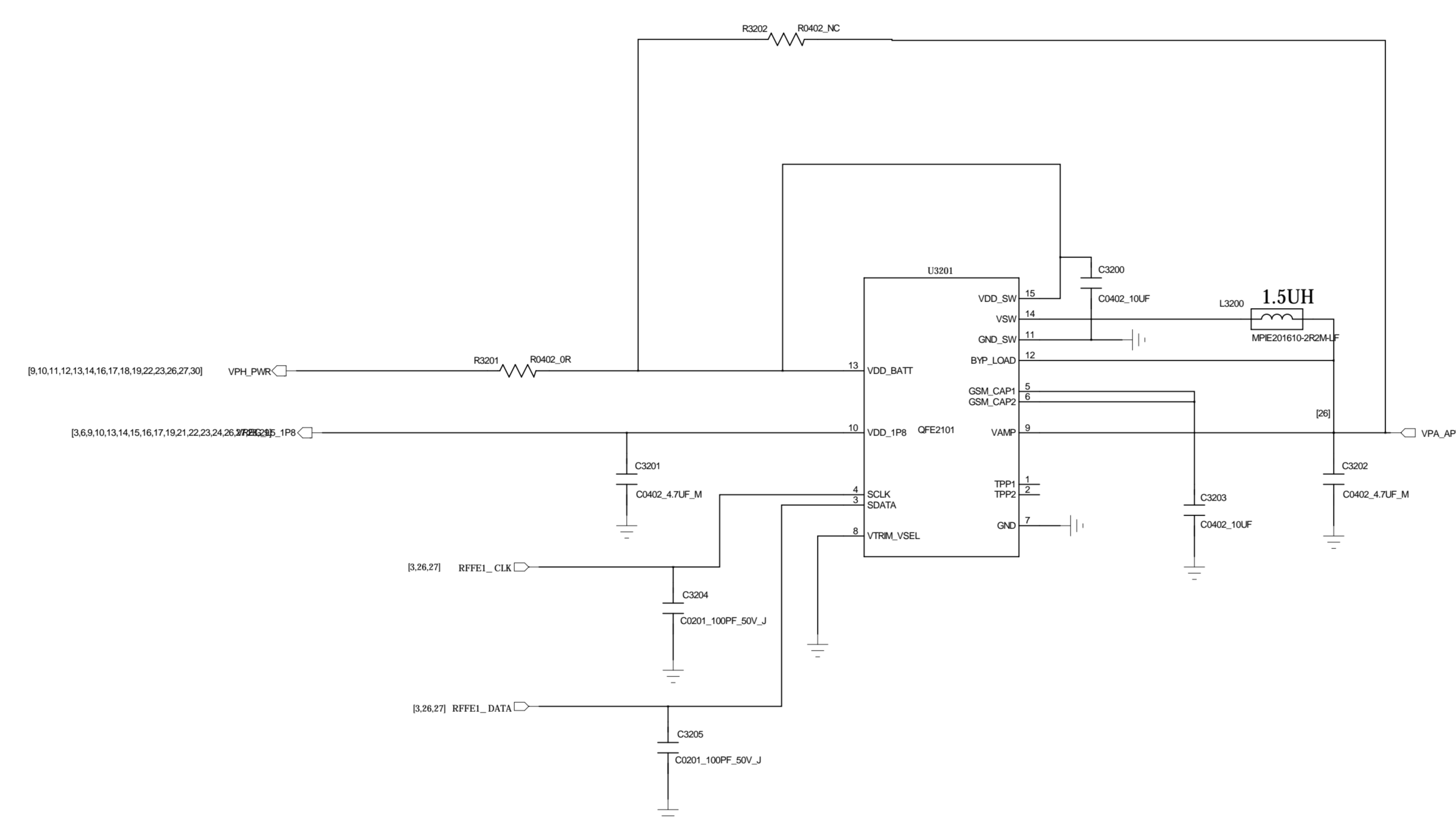


	eINA option	Non-eINA option
R4902	DNI	0ohm
R4904	0ohm	DNI
R4903	DNI	0ohm
C4903	33pF	DNI
FL4902	SAFFB1G56KB0P0A	P6QA1G582H2JM0S

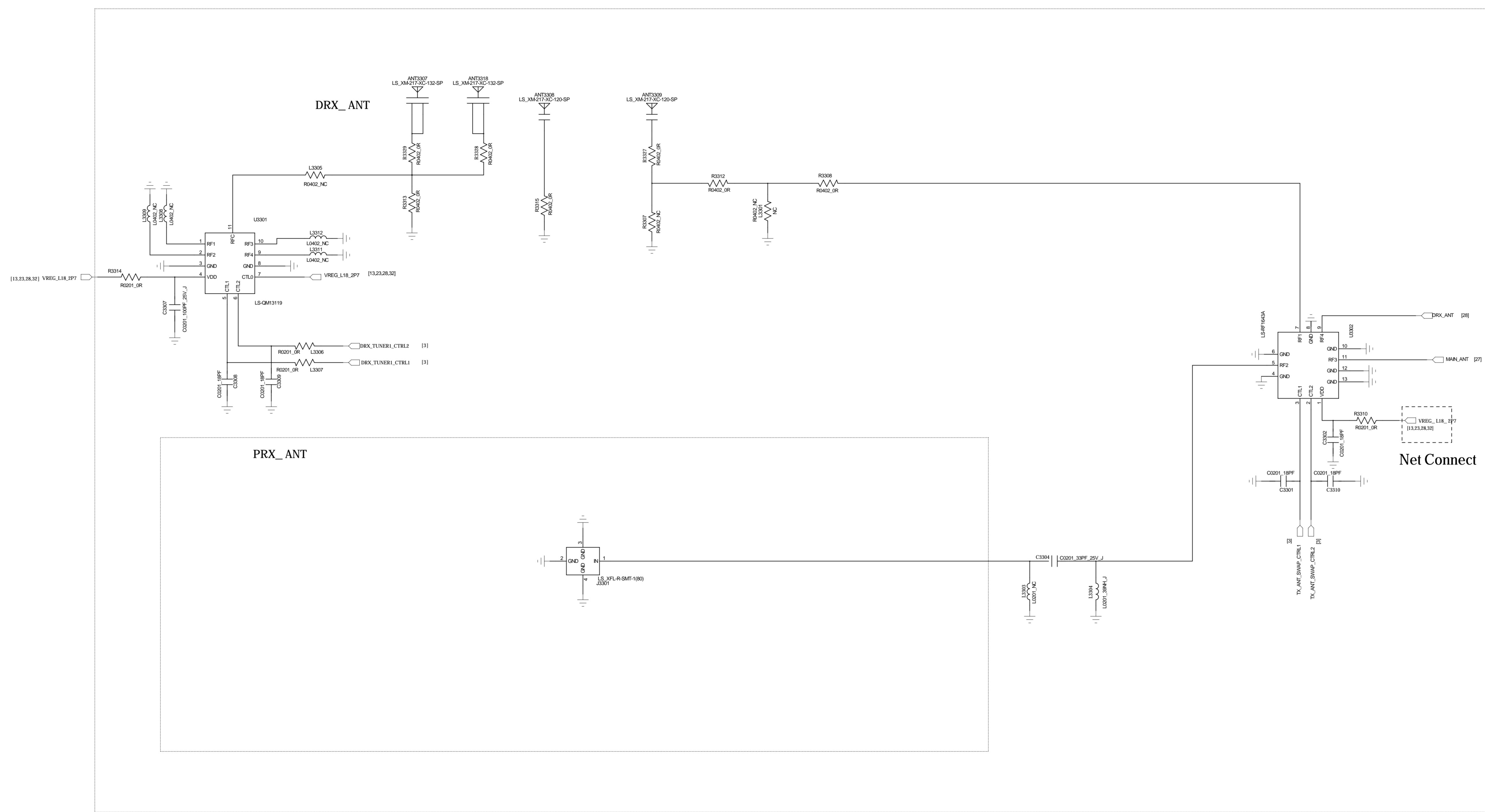
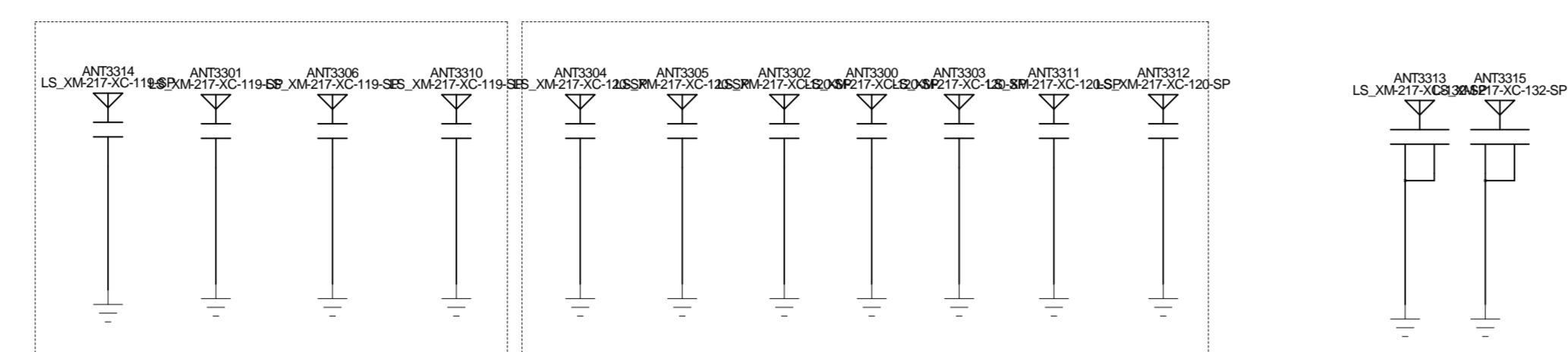


COMPANY: <Company Name>			
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REVISION RECORD			
LTN	ISSNO	APPROVED	DATE



REVISION RECORD			
LR	RECORD	APPROVED	DATE



DRAWN: <Drawn By>				DATED: <Drawn Date>			
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RELEASED: <Released By>				DATED: <Release Date>			

COMPANY: <Company Name>	
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